Center for Energy Efficient Electronics Science

Searching for the Milli-Volt Switch

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Winton Inaugural Symposium on Energy Efficiency

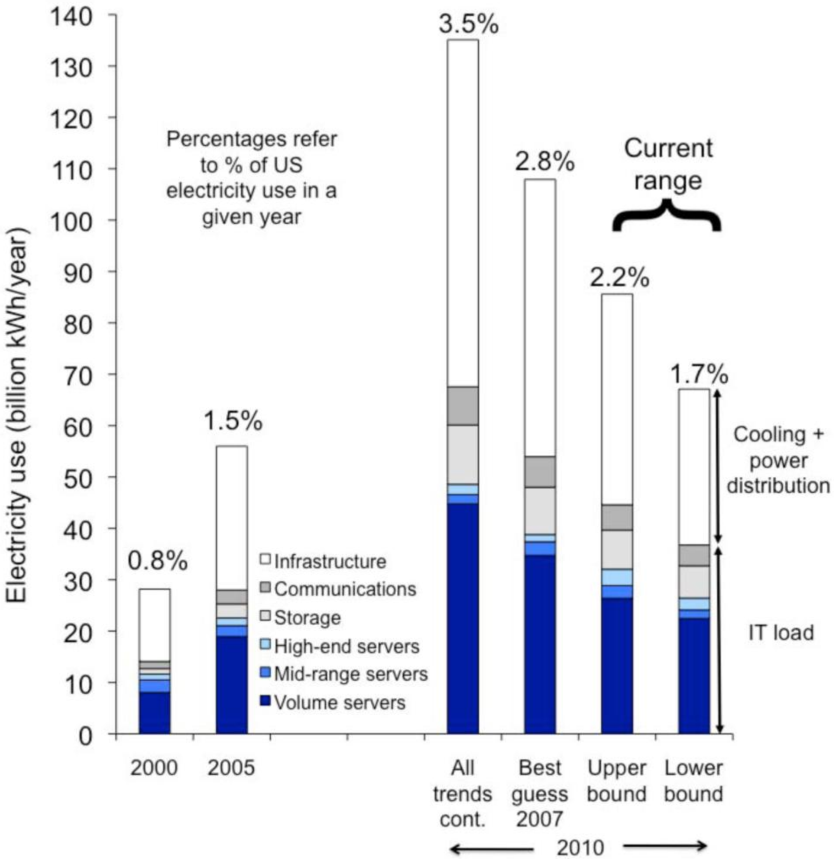
Cambridge, United Kingdom

Oct. 1, 2012

Contra Costa-UC Berkeley-MIT-LATTC-Stanford-Tuskegee

A Science & Technology Center

Data Center Electricity Usage



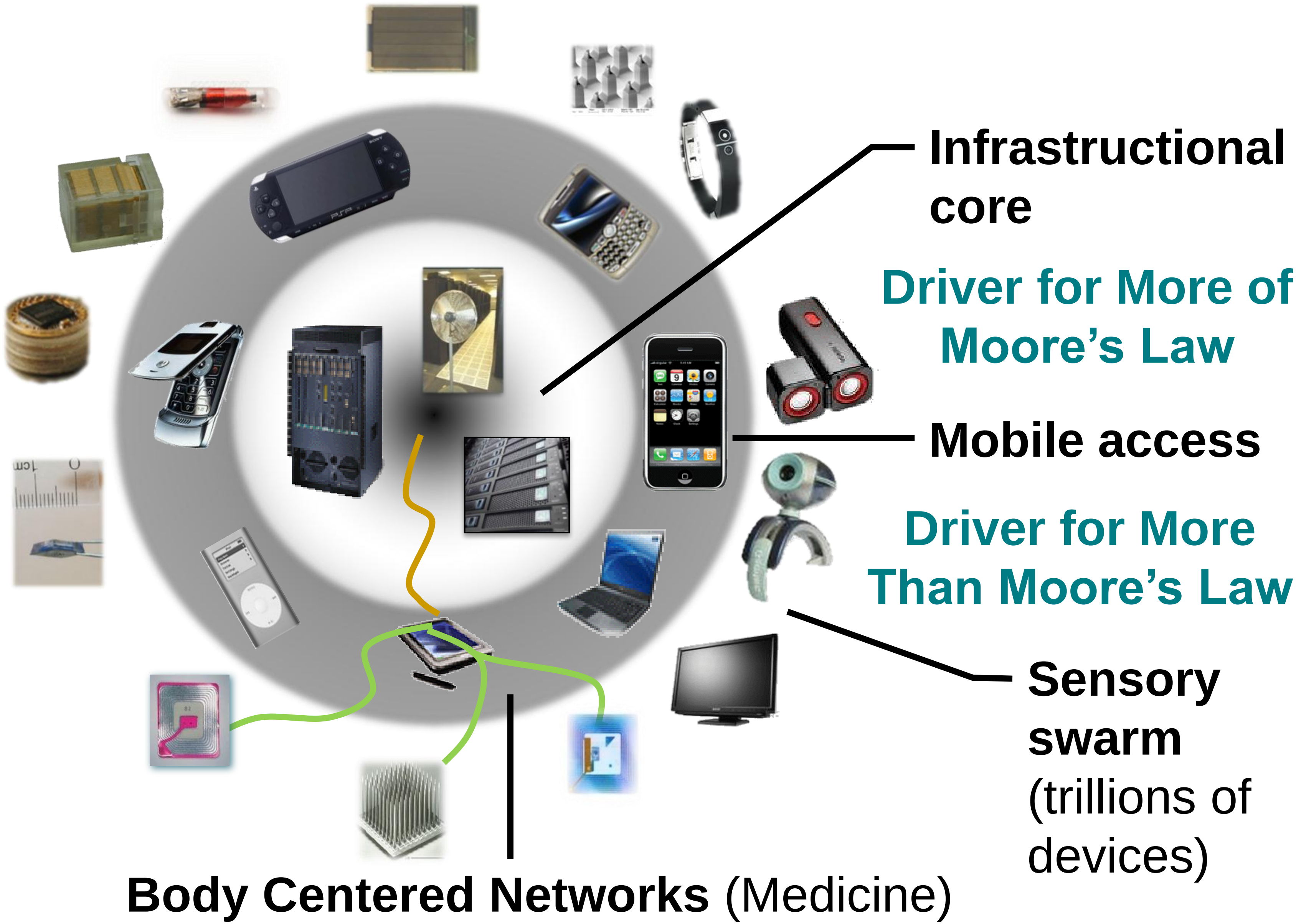
In 2010, data centers accounted for
~1.3% of all electricity use worldwide,
~2% of all electricity use in the U.S.

Google

Google's new data center in Hamina, Finland, has an energy-efficient cooling system that uses seawater from a nearby bay.

J. Koomey, *Growth in Data center electricity use 2005 to 2010* (Analytics Press, Oakland, CA), 201

Vision for 2020: Swarms of Electronics:



Power Usage Rising Faster Than Past Trend

- **Because power consumption $\propto V_{dd}^2$ and V_{dd} (operation voltage) scaling has slowed after 0.13µm node.**

Technology Node			**0.25 µm**	**0.18 µm**	**0.13 µm**	**90 nm**	**65 nm**	**45 nm**	**32 nm**	**22 nm**	**16 nm**
V_{dd}			**2.5 V**	**1.8 V**	**1.3 V**	**1.2 V**	**1.1 V**	**1.0 V**	**0.9 V**	**0.8 V**	**0.7 V**

High Performance ITRS Roadmap

What is the energy cost of reading out your flash memory?

Read the current going through a resistor, in the presence of noise:

$$(\Delta i)^2 = 2q\, i \times \Delta f \ldots\ldots\ldots \text{Shot Noise}$$

$$(\Delta i)^2 = \frac{4kT}{R} \times \Delta f \ldots\ldots\ldots \text{Johnson Noise}$$

$$\text{Required voltage } V = iR >> 2kT/q \sim 50\text{mVolts}$$

$$\text{Signal-to-Noise Ratio} = \frac{i}{\sqrt{2q\, i\Delta f}} = \sqrt{\frac{i}{2q\, \Delta f}}$$

$$i > 2q \times \Delta f$$

$$\text{Required power } iV > 2q\, \Delta f \times \frac{2kT}{q} = 4kT \times \Delta f$$

With a safety margin:

$$\text{Energy Consumed} \sim 40\text{ kT per bit processed}$$

Units:

~40kT/bit of information

0.16 atto-Joules/bit of information

0.16 nano-Watts/Gbit/second

This is about 10^6 times less energy than we are using today!

What will be the energy cost, per bit processed?

1. Logic energy cost ~40kT per bit processed

2. Storage energy cost ~40kT per bit processed

3. Communications currently >100,000kT per bit processed

.

There are many type of memory possible:

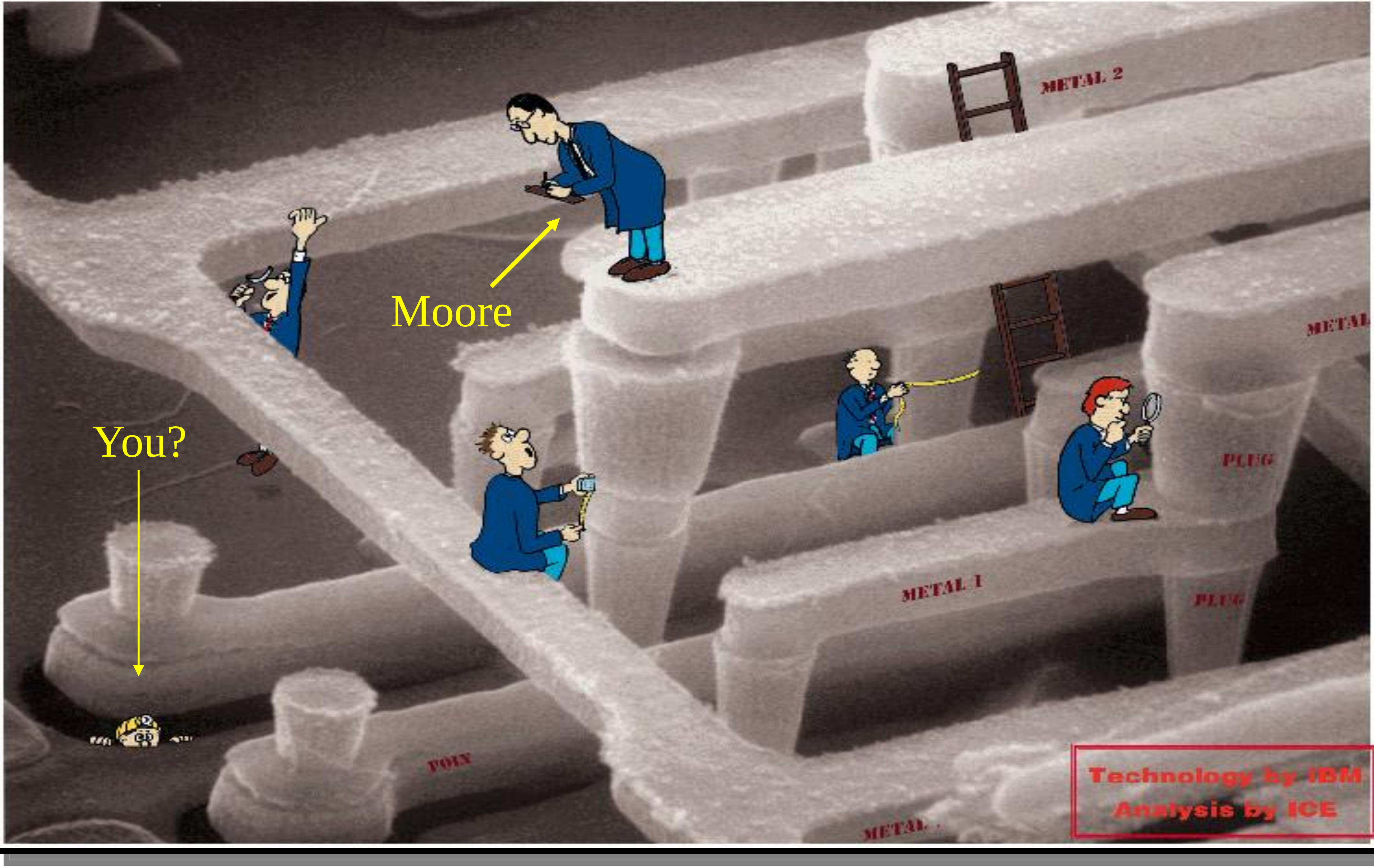
1. Flash
2. SRAM
3. Dram
4. Magnetic Spin
5. Nano-Electro-Chemical Cells
6. Nano-Electro-Mechanical NEMS
7. Memristor
8. Chalcogenide glass (phase change)
9. Carbon Nanotubes

   -
   -

Similarly there are many ways to do logic.

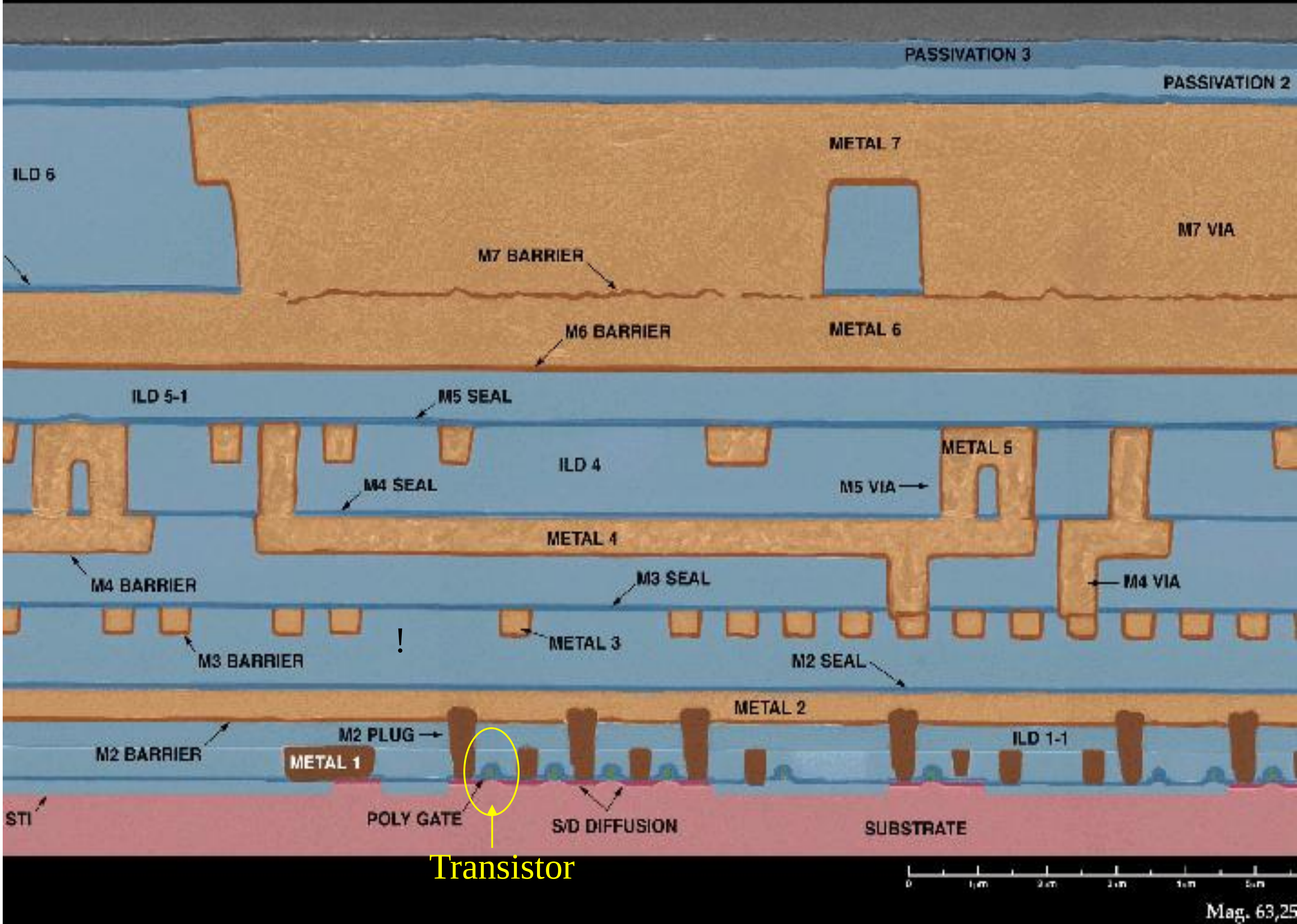
But there are not many ways to communicate:

1. Microwaves (electrical)
2. Optical



METAL 2
Moore
METAL
You?
PLUG
METAL 1
PLUG
POLY
METAL
Technology by IBM
Analysis by ICE

IBM's Power PC750 Microprocessor



What is the energy cost for electrical communication?

$$V_{noise}^2 = 4kT\,R\,\Delta f$$

$$\frac{V_{noise}^2}{R} = 4kT\ \Delta f$$

$$\begin{array}{c}\text{Signal}\\ \text{Energy}\end{array} \geq \begin{array}{c}\text{Noise Power}\\ \text{per bit}\end{array} = 4kT \text{ per bit}$$

All information processing costs ~ $40kT$ per bit.

(for good Signal-to-Noise Ratio)

Great!

So what's the problem?

The natural voltage range for wired communication is rather low:

$$V_{noise}^2 = 4kT\,R\,\Delta f$$

$$V_{noise}^2 = 4kT\,R\,\frac{1}{RC}$$

$$V_{noise}^2 = 4kT \times \frac{1}{C}$$

$$V_{noise}^2 = \frac{4kT}{q} \times \frac{q}{C}$$

$$V_{noise} = \sqrt{\underbrace{4kT/q}_{100\text{mVolts}} \times \underbrace{q/C}_{10\mu\text{Volts}}}$$

$$V \approx 1\,\text{mVolt}$$

The natural voltage range for a thermally activated switch like transistors is >>kT/q, eg. ~ 40kT/q or about ~1Volt

Voltage Matching Crisis at the nano-scale!

If you ignore it the penalty will be $(1\text{Volt}/1\text{mVolt})^2 = 10^6$

The wire wants 1000 electrons at 1mVolt each.

(to fulfill the signal-to-noise requirement >1eV of energy)

The thermally activated device wants at least one electron at ~1Volt.

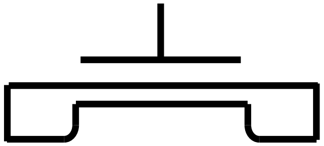
The New Switch has to Satisfy Three Specifications:

1. Steepness (or sensitivity)
switches with only a few milli-volts
60mV/decade $\Rightarrow$ **1mV/decade**

2. On/Off ratio. $10^6 : 1$

3. Current Density or Conductance Density
(for miniaturization)
old spec at 1Volt: 1 mAmp/micron
our spec: **1 milli-mho/micron**

A low-voltage technology, or an impedance matching device, needs to be invented/discovered at the Nano-scale:



transistor amplifier with
steeper sub-threshold slope

- TFET's
- Negative Capacitance Gates

--VO_2 metal-insulator transition

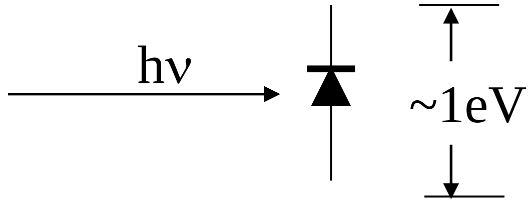
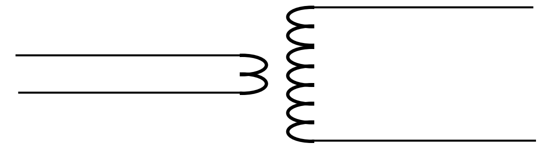
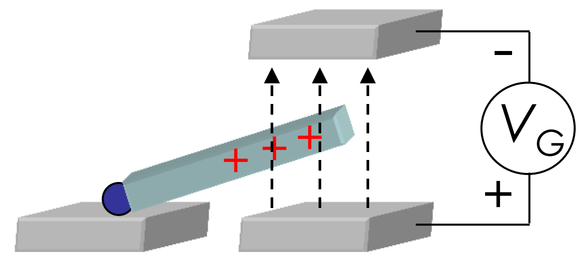


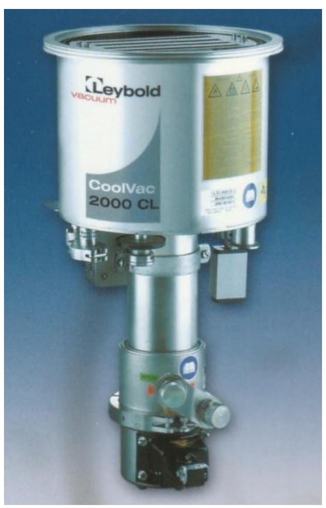
photo-diode



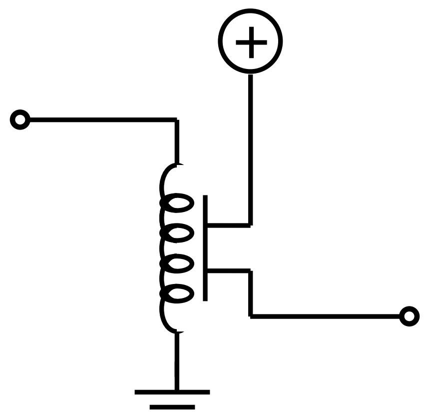
nano-transformer



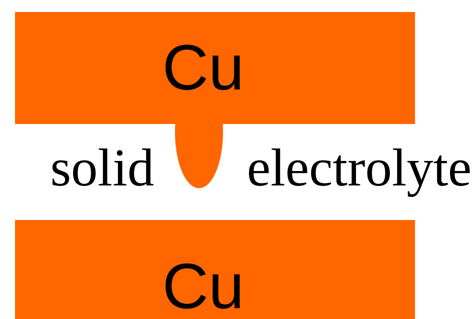
MEM's switch



Cryo-Electronics
kT/q~q/C

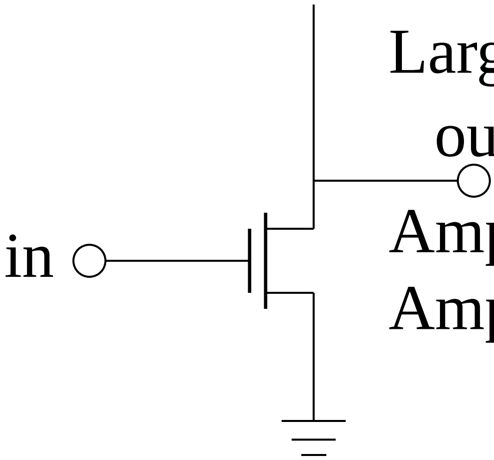


giant magneto-resistance
spintronics



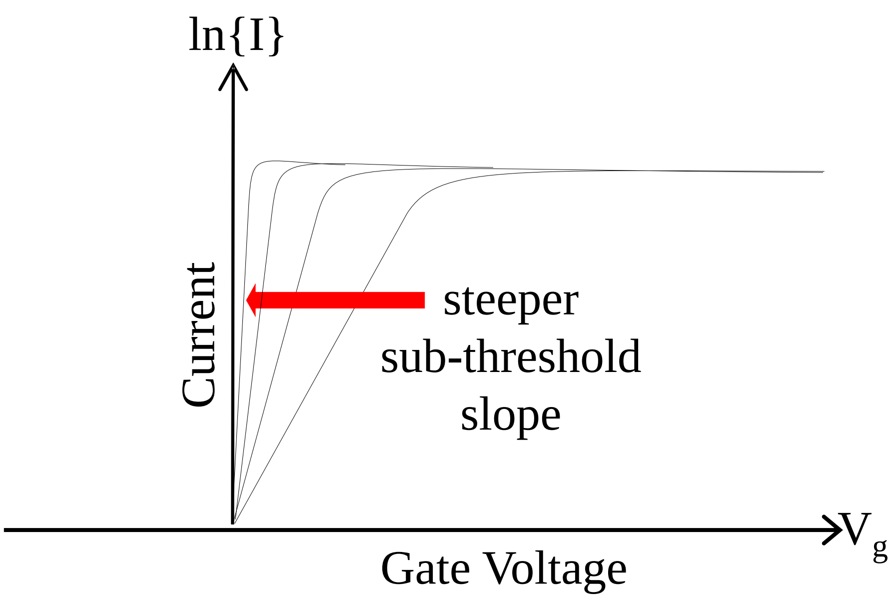
Electro-Chemical Switch

An amplifying transistor as a voltage matching device:

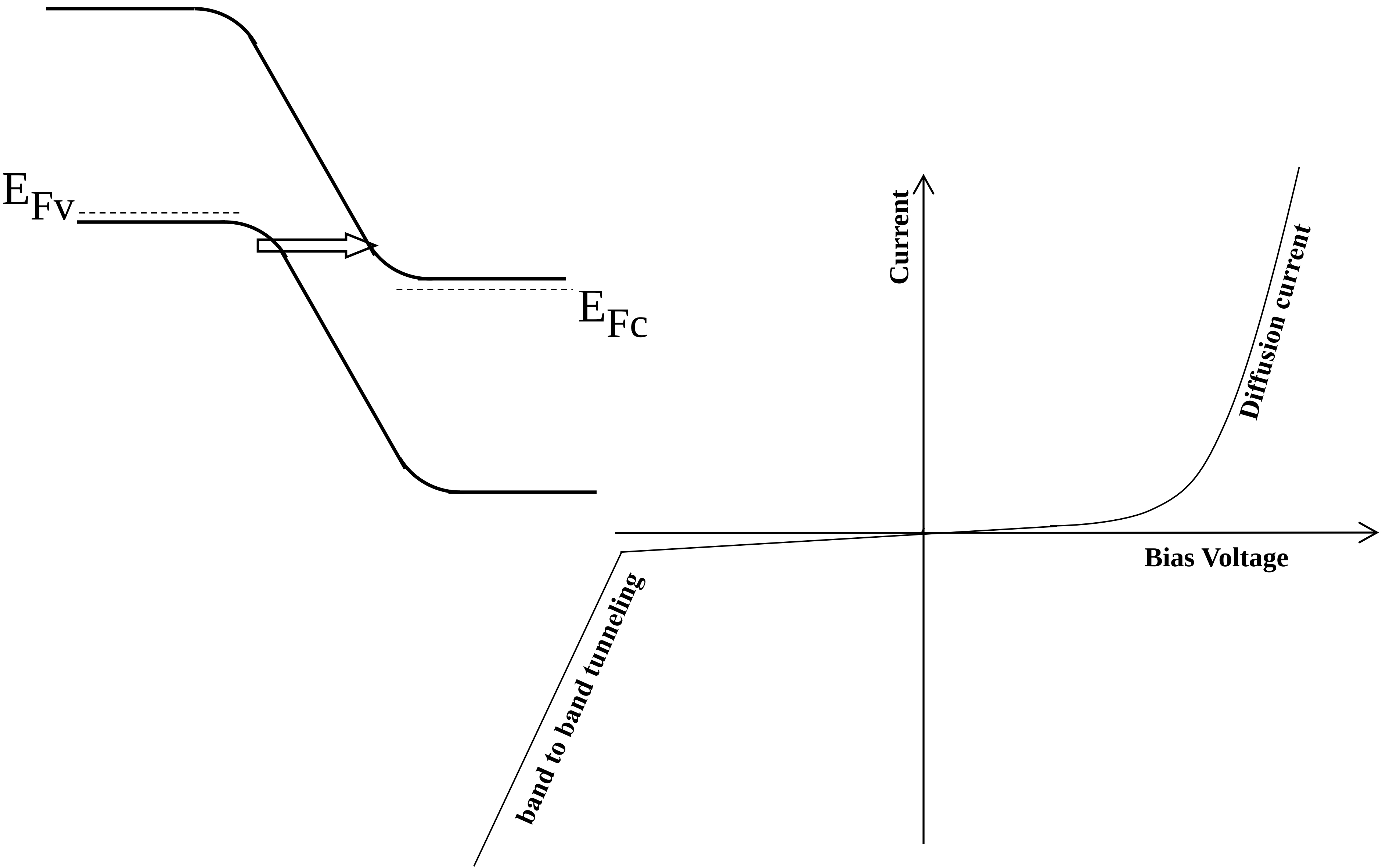


Small voltage in
Large voltage out

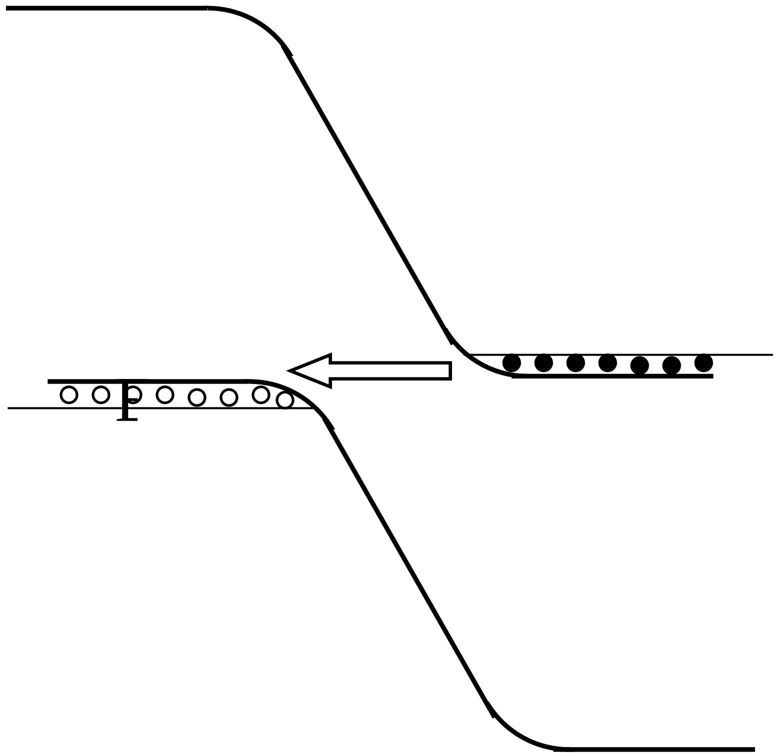
Amplification of weak signals has an energy cost!
Amplification of weak signals has a speed penalty!

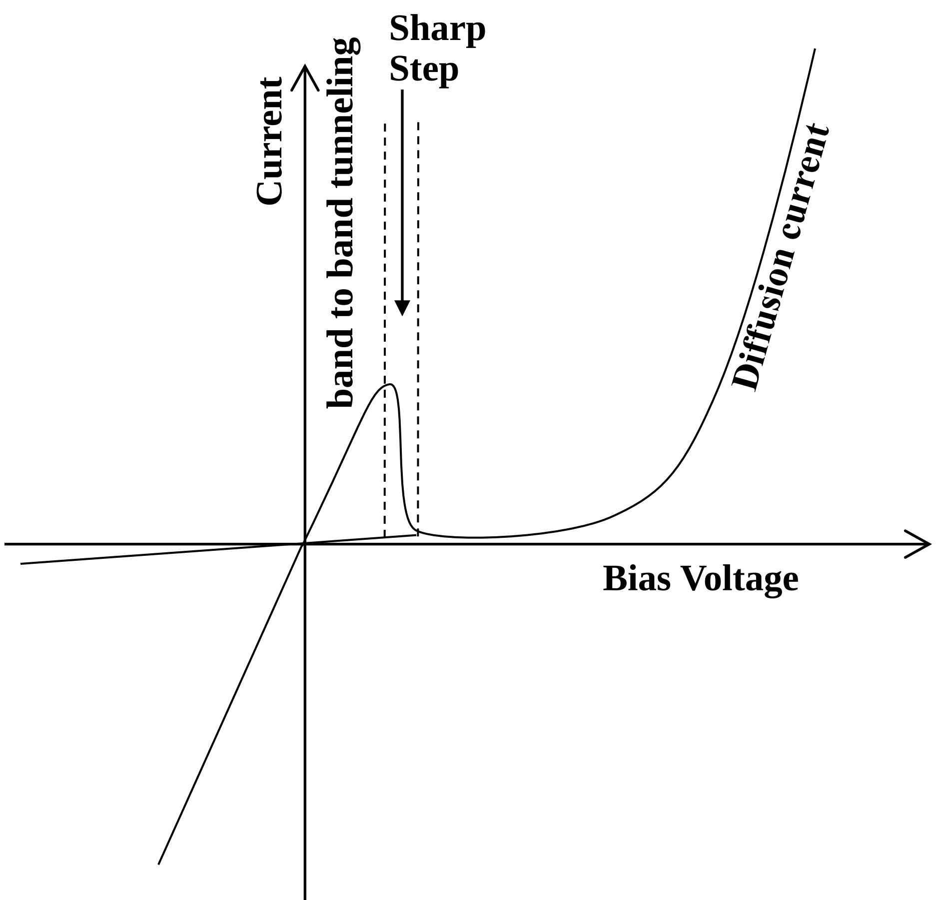


The Zener Diode:

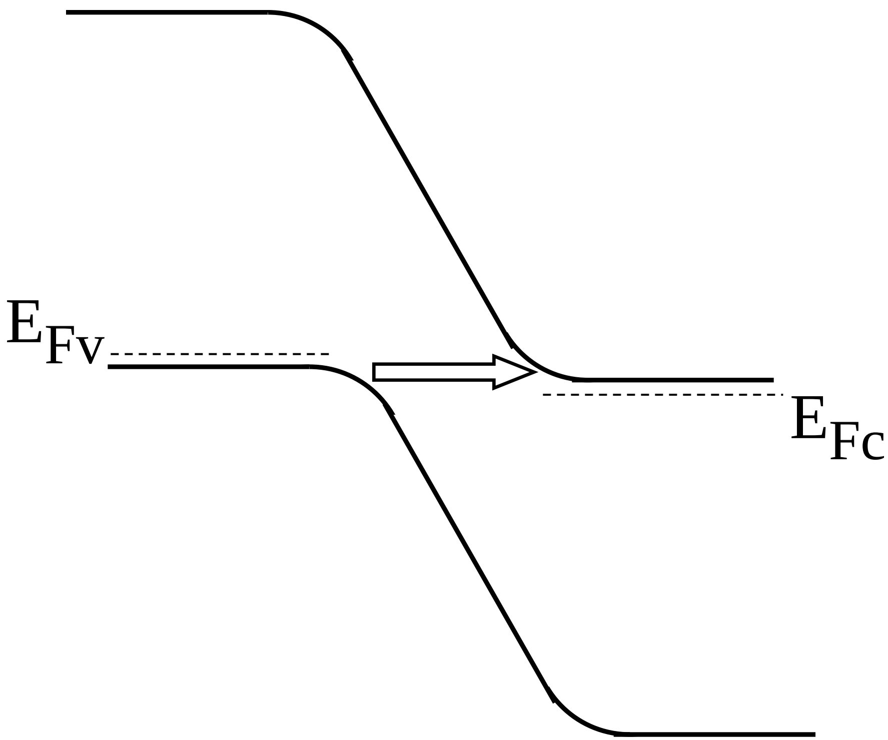


The Esaki Diode:

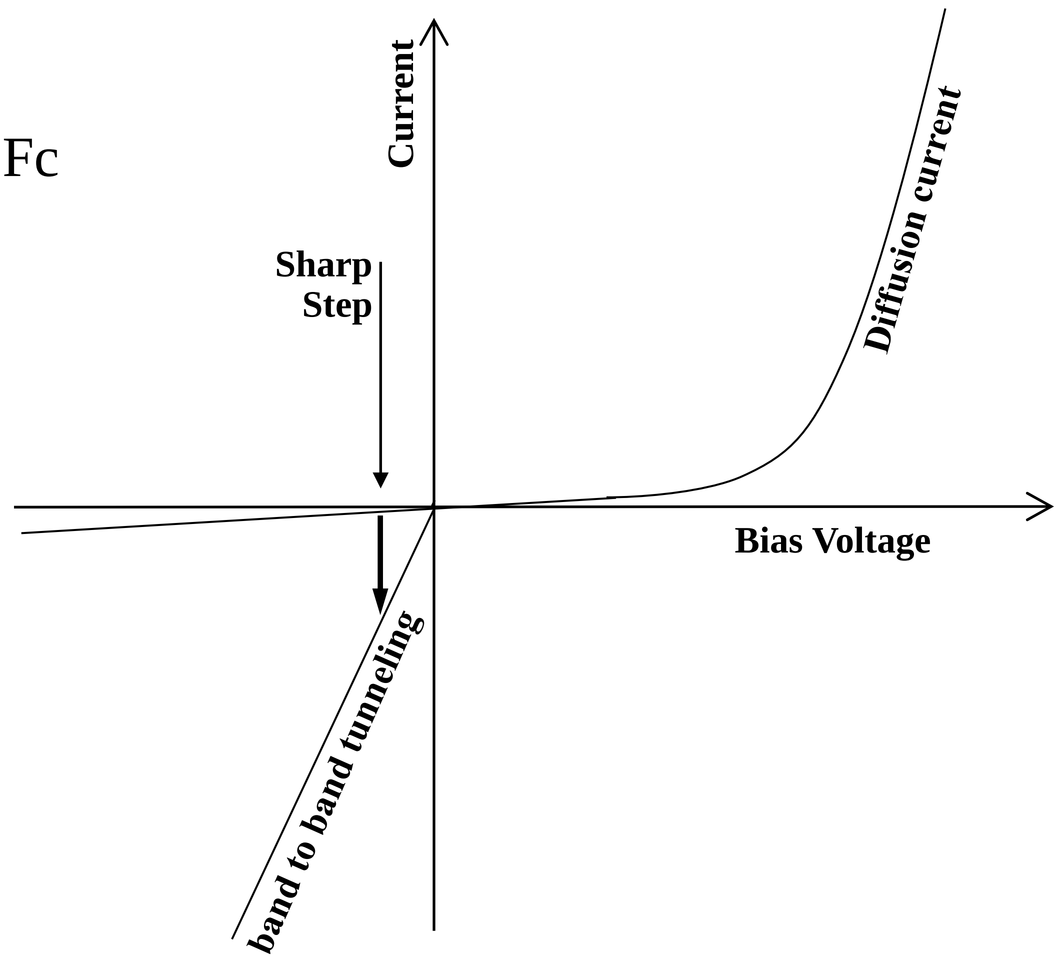




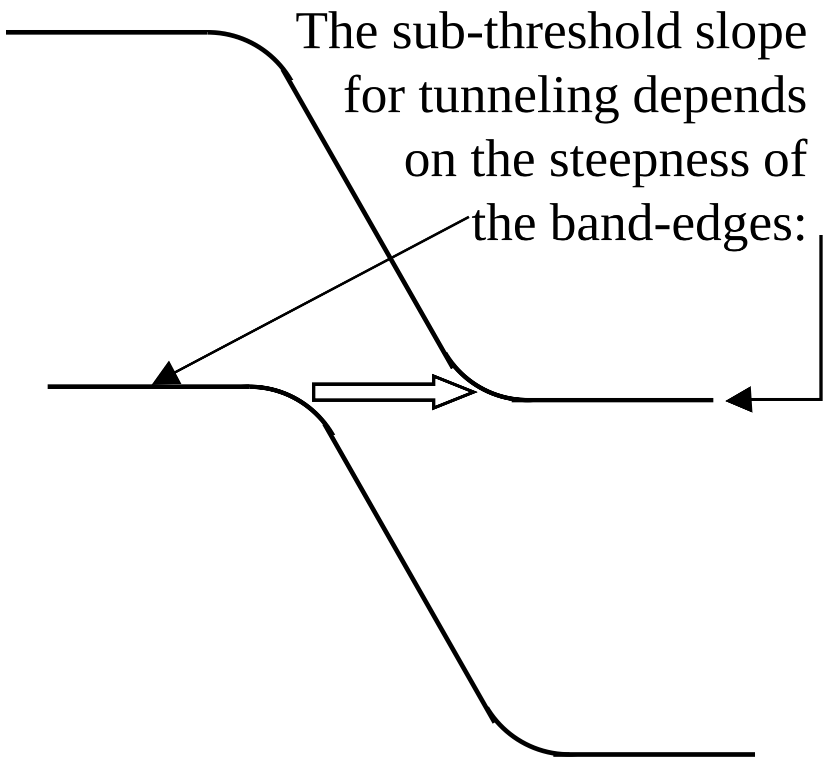
The Backward Diode as a Switch:



<u>The Backward Diode:</u>
These have been routinely made in Ge homo-junctions, since the 1960's.

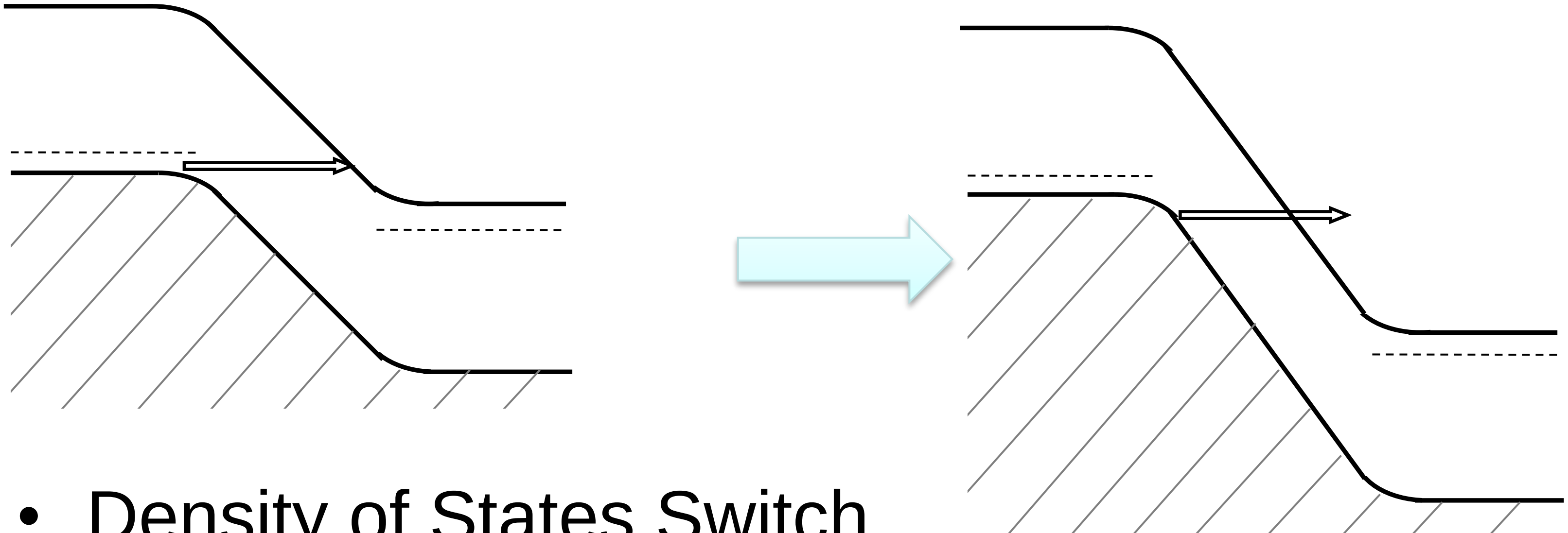


The Backward Diode as a Switch:

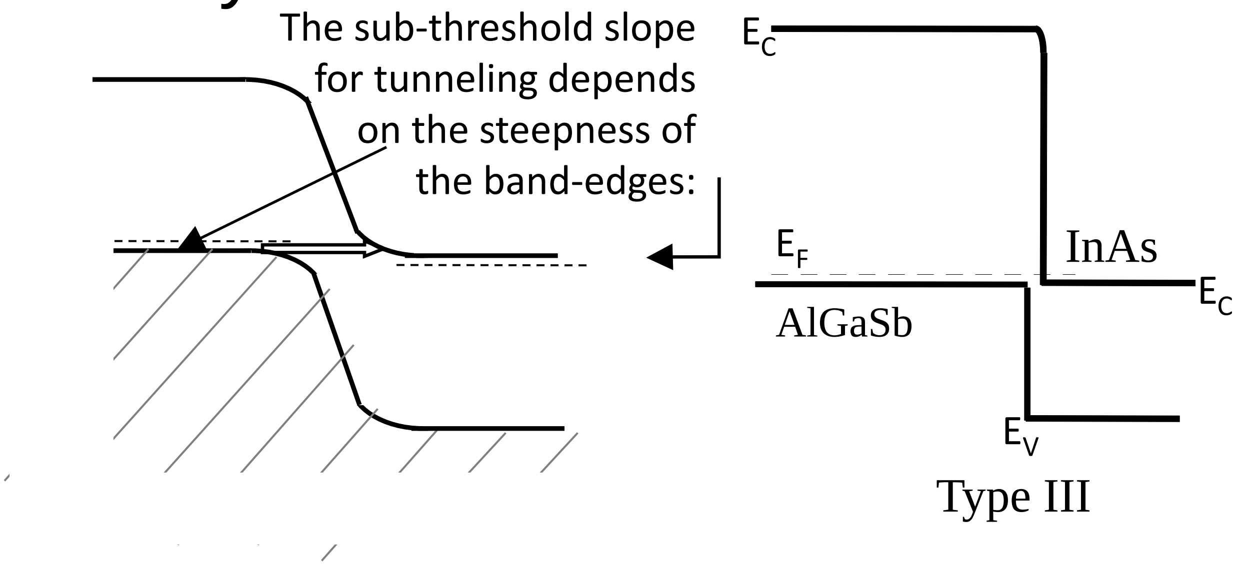


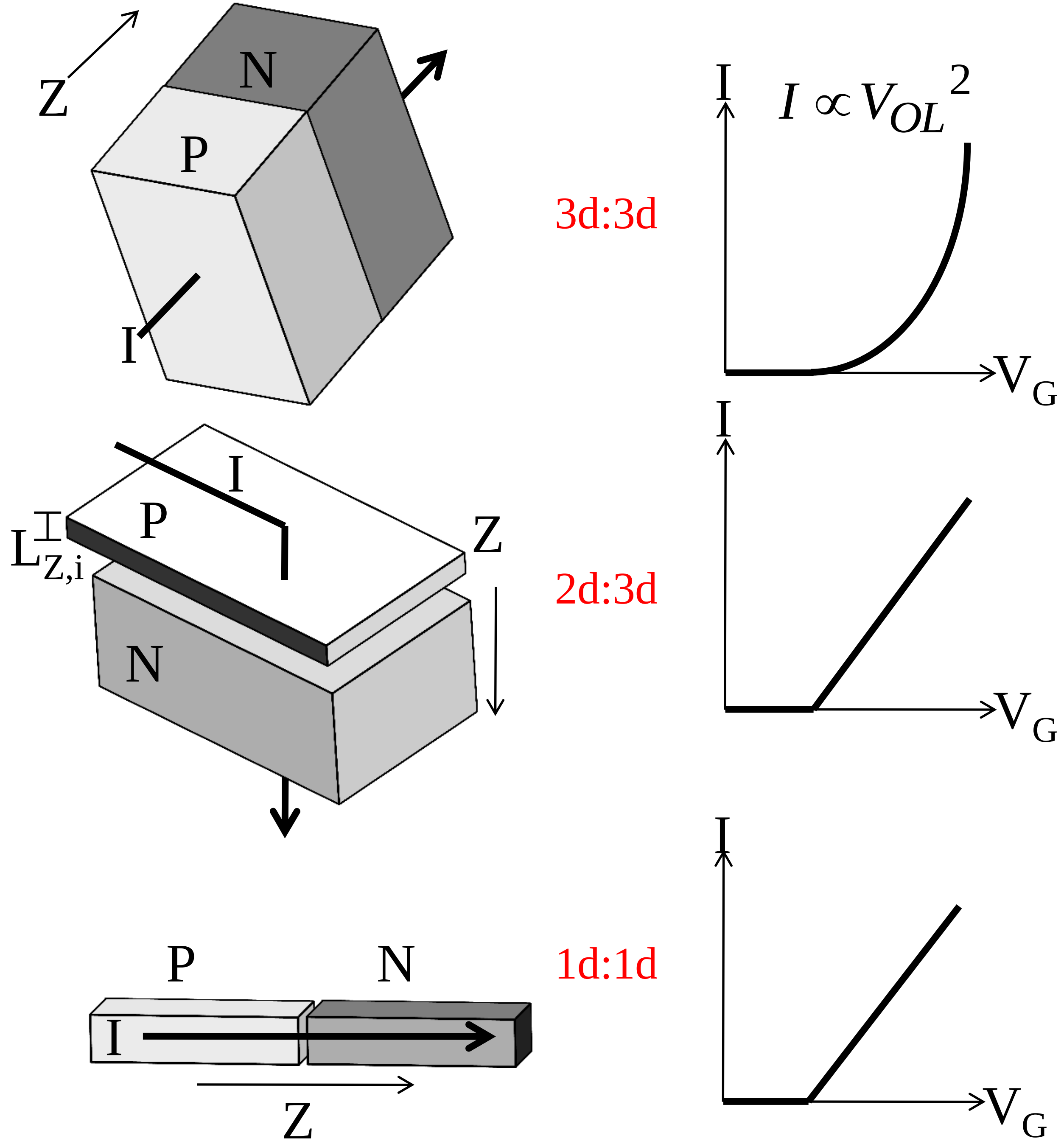
2 Ways to Obtain Steepness:

- Modulate the Tunneling Barrier:

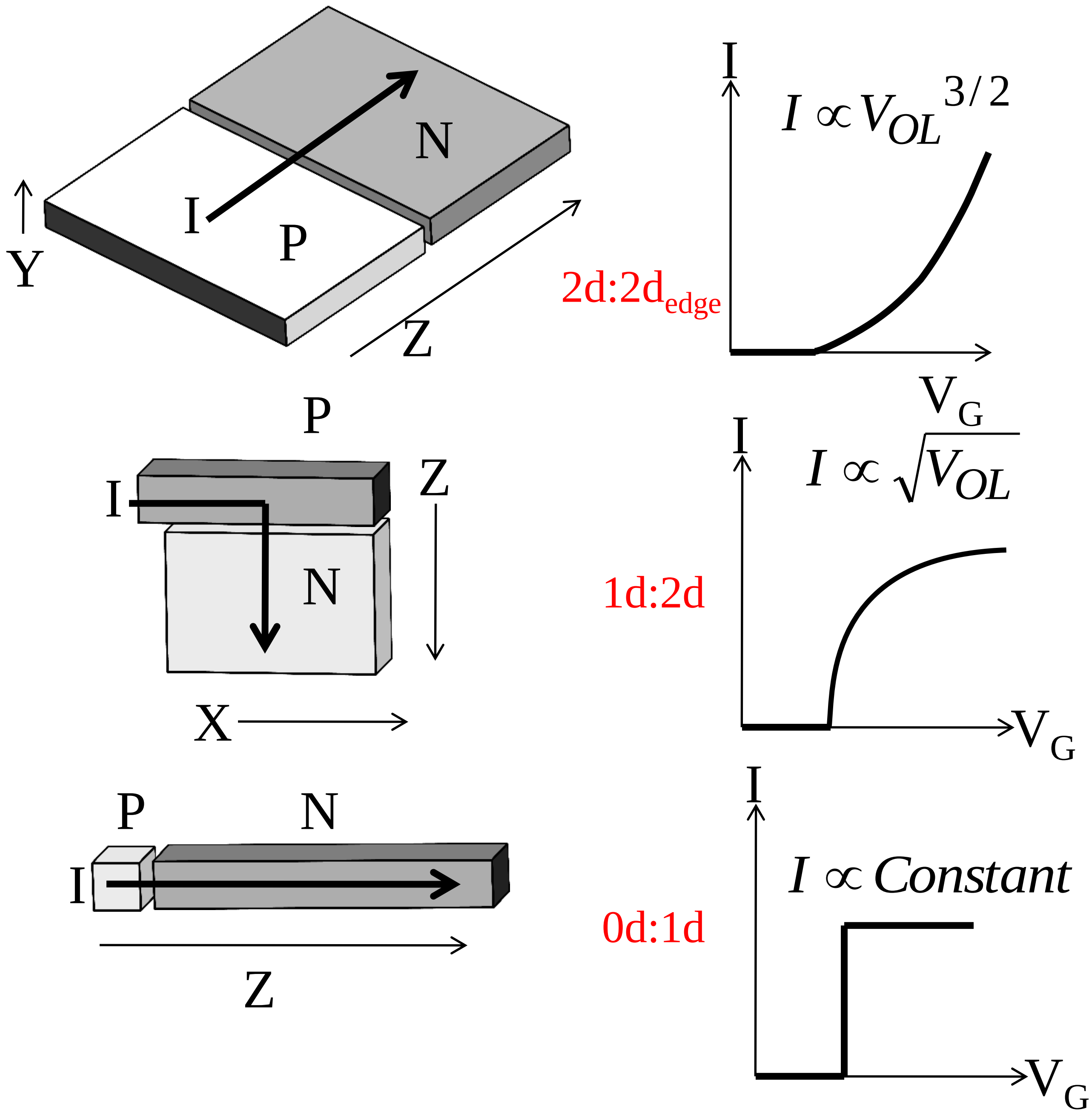


- Density of States Switch

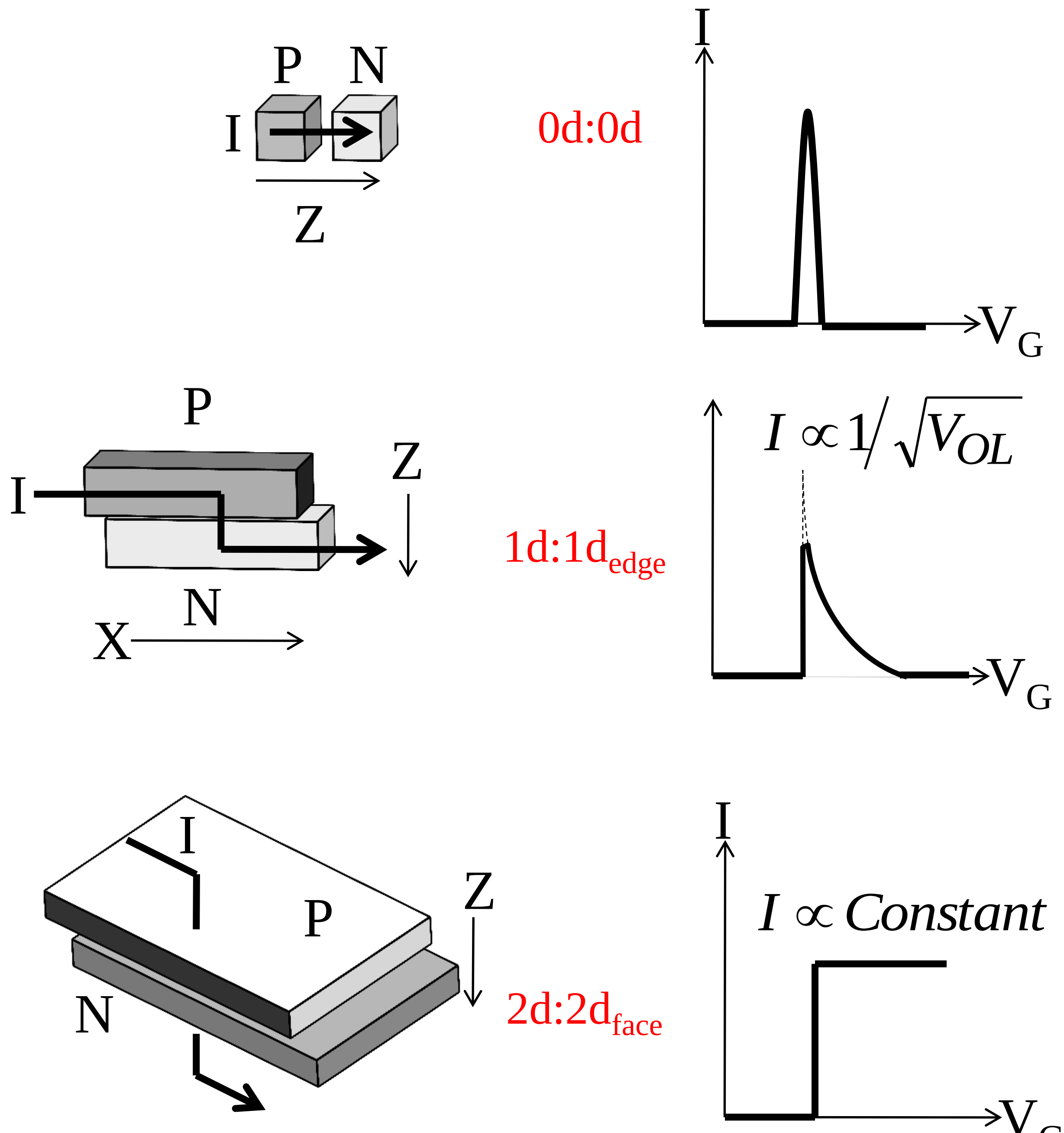




Z
N
P
I
3d:3d
I
$I \propto V_{OL}^{2}$
V_G
I
P
$L_{Z,i}$
Z
N
2d:3d
I
V_G
P
N
I
Z
1d:1d
I
V_G

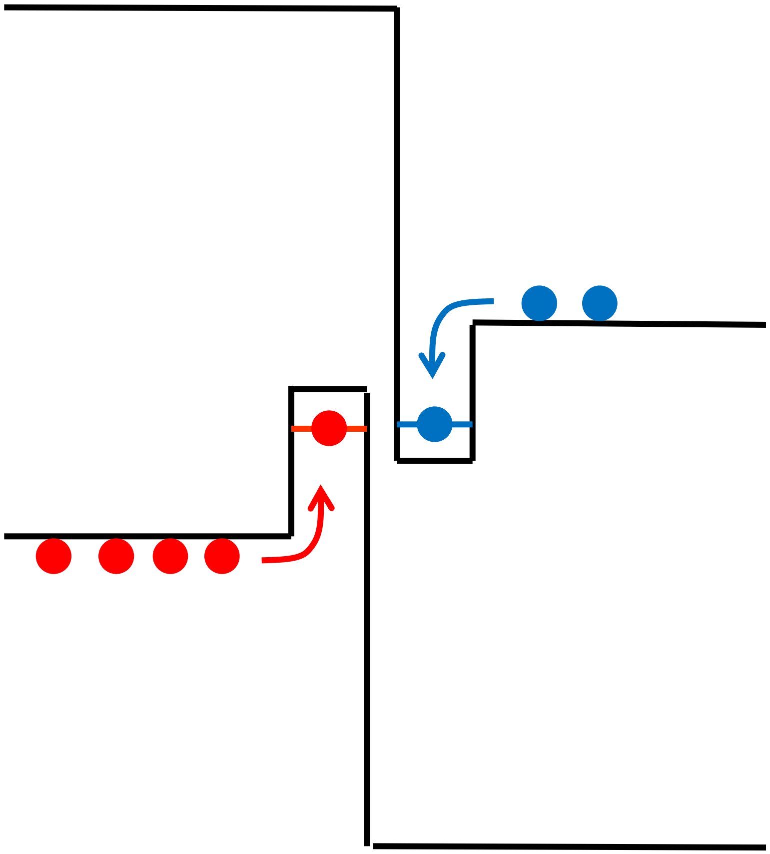


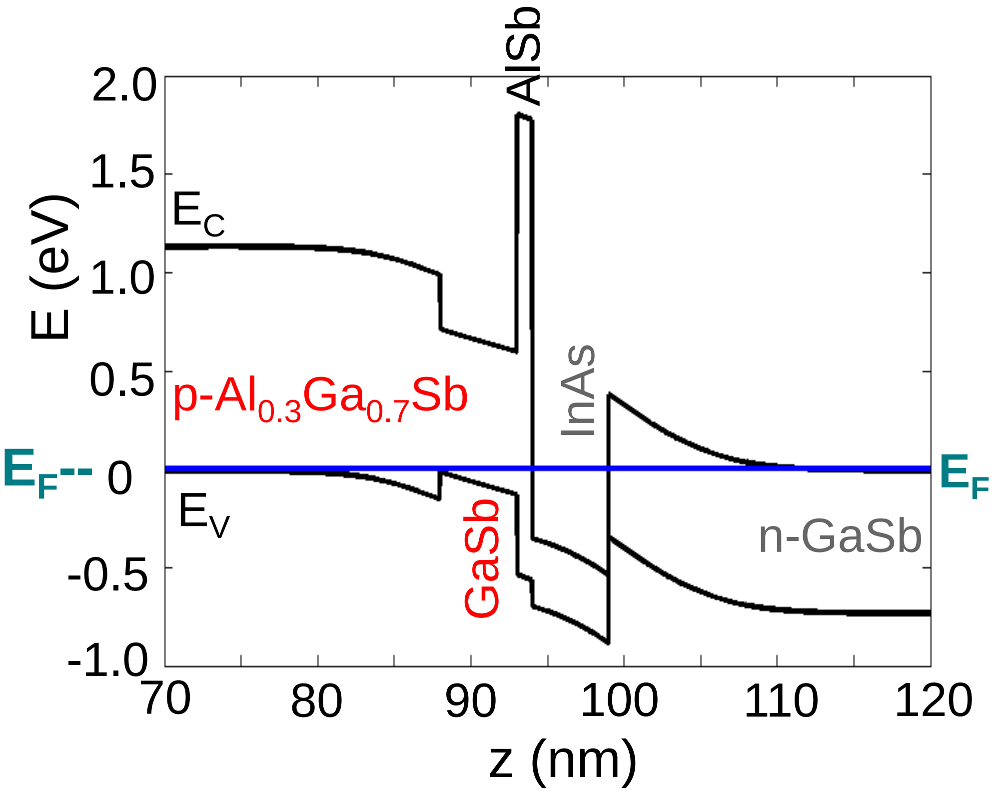
I
P
N
Y
Z
2d:2d$_{edge}$
$I \propto V_{OL}^{3/2}$
V_G
P
I
Z
N
X
1d:2d
$I \propto \sqrt{V_{OL}}$
P
N
I
Z
0d:1d
$I \propto Constant$

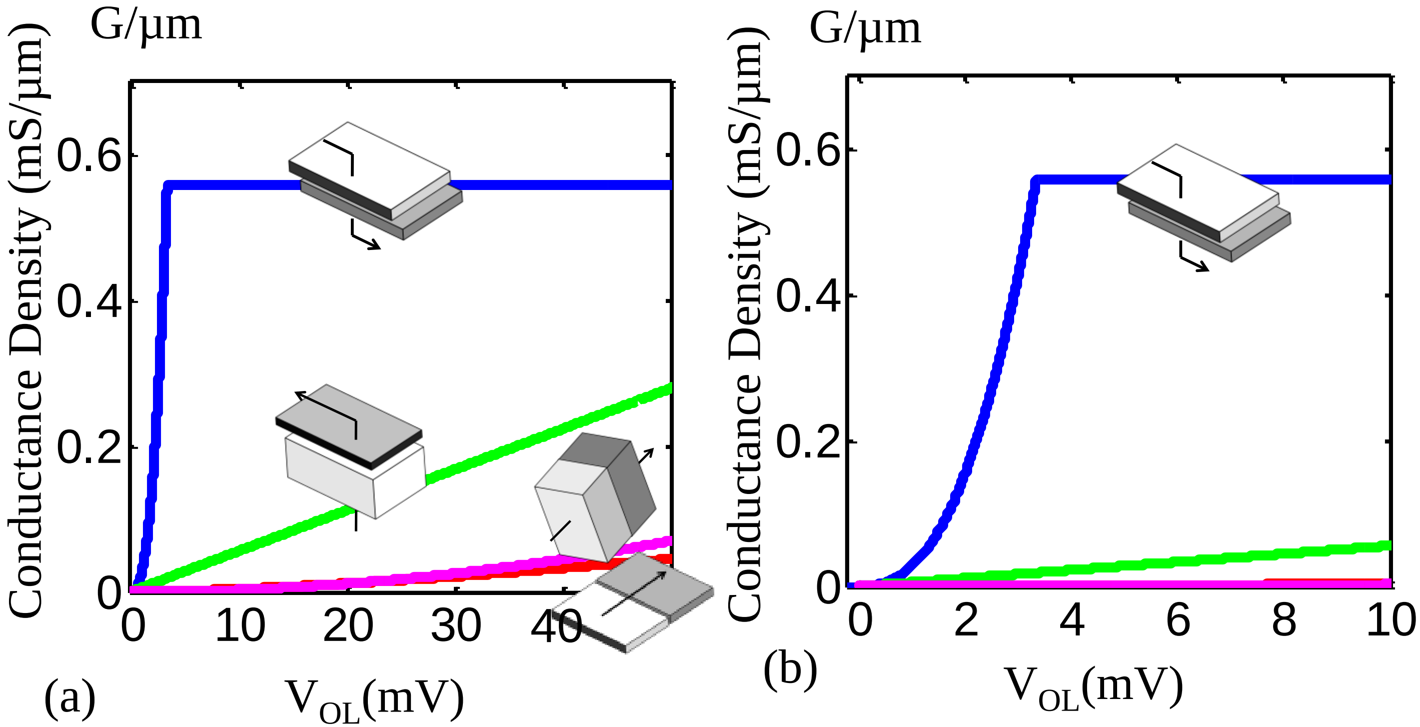

P
N
I
Z
0d:0d
I
V G
P
Z
I
N
X
1d:1dedge
$I \propto 1/\sqrt{V_{OL}}$
V G
I
Z
P
N
2d:2dface
I
$I \propto Constant$
V G

Type III band alignment

Idealized structure





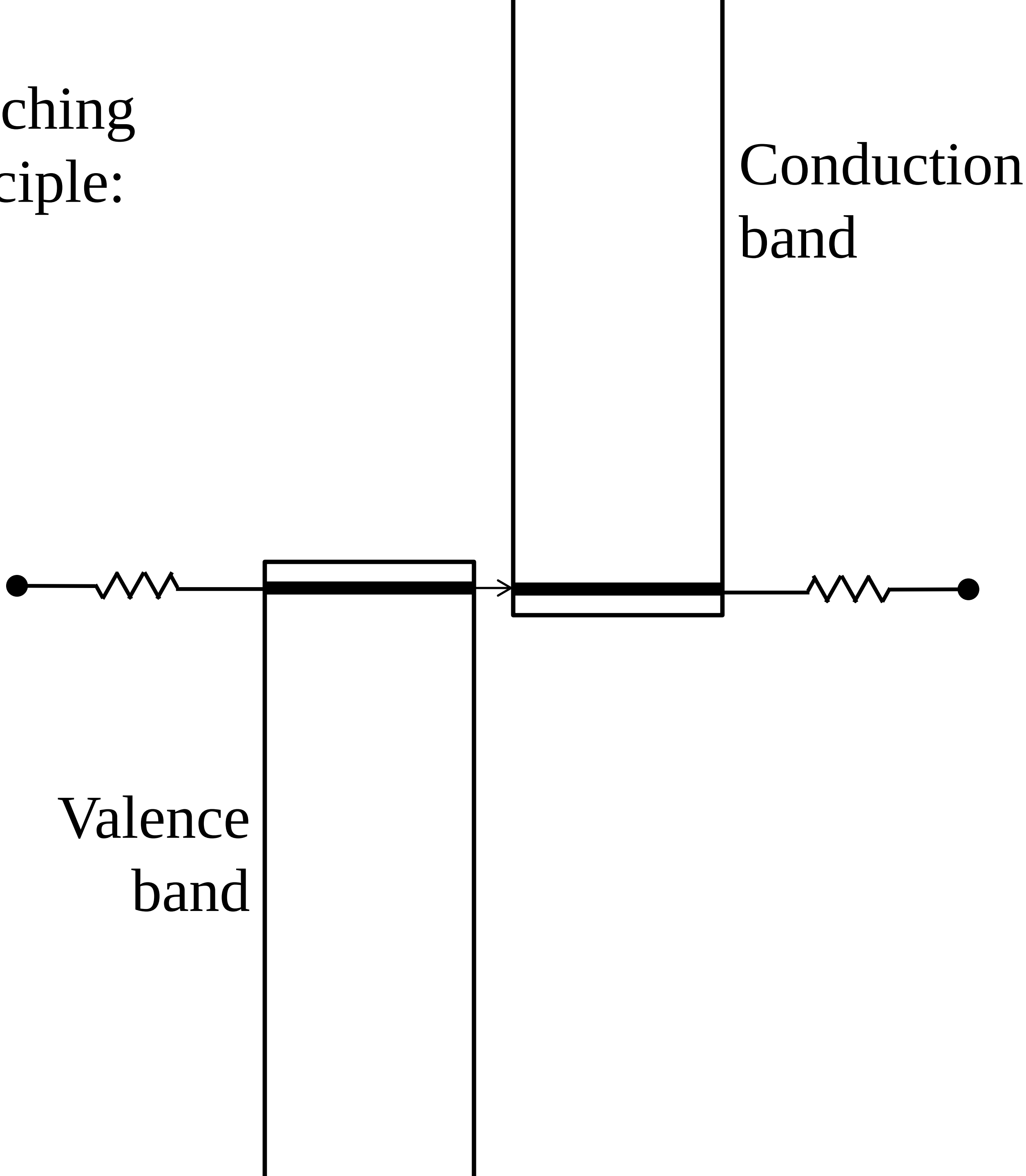


γ=2.34 meV
E_Z=50 meV

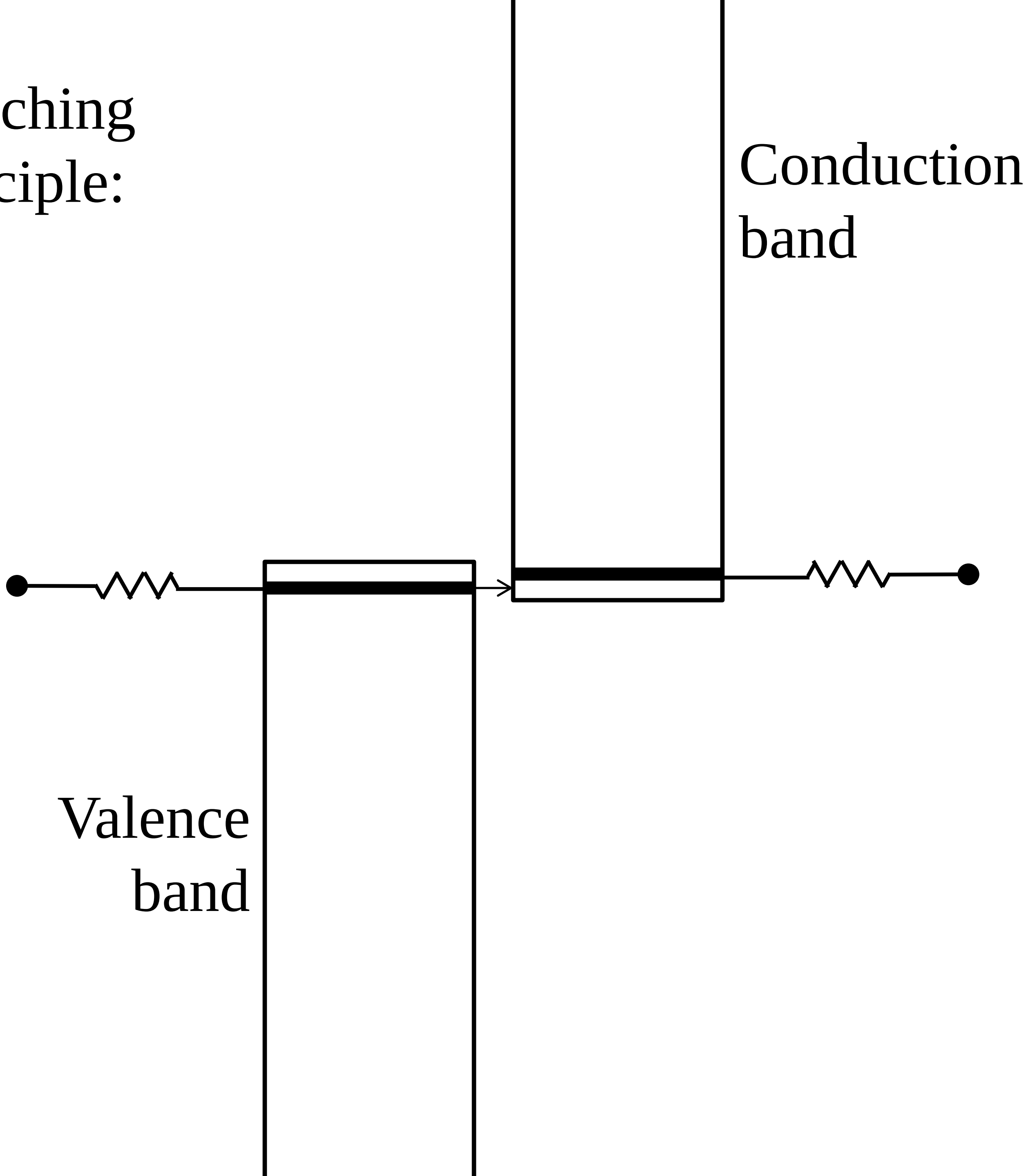
$\mathcal{T}_{device}$=2.16%
L_X=32 nm
L_Z=8.672 nm

m*=0.1

Switching Principle:

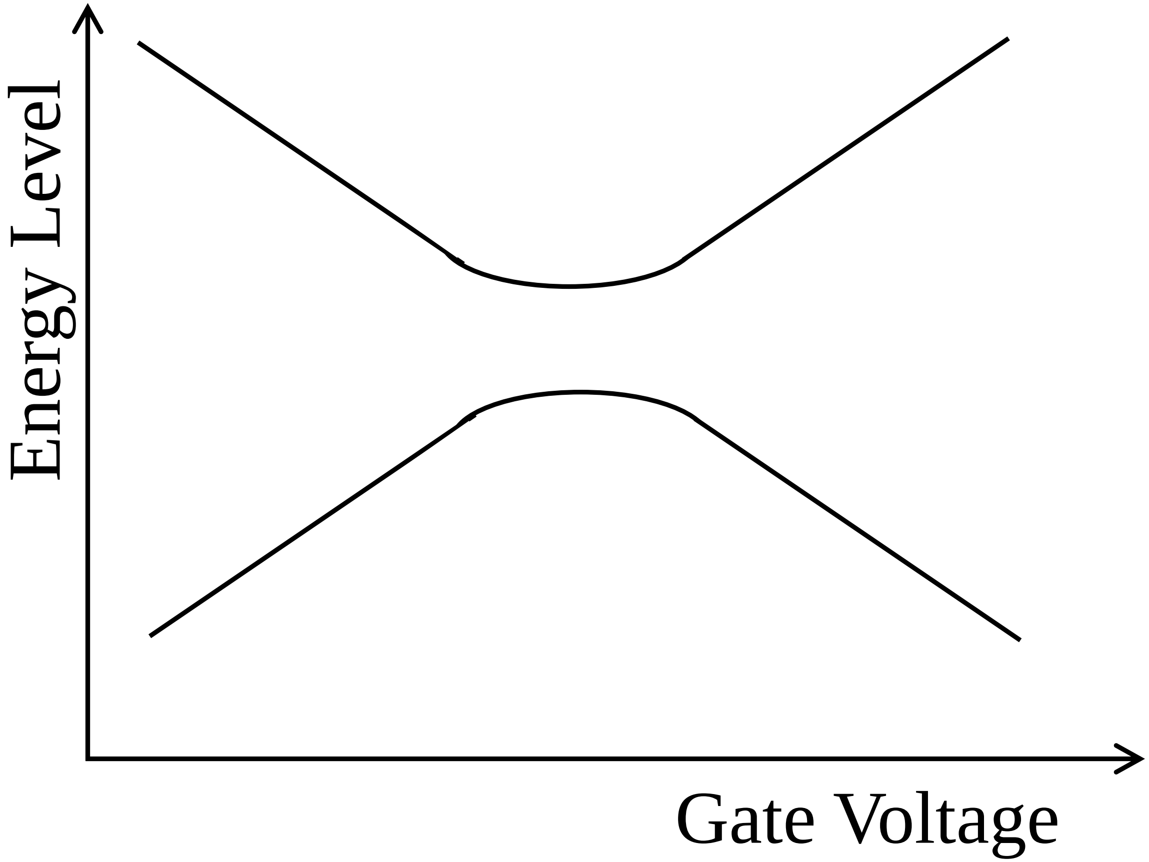


Switching Principle:



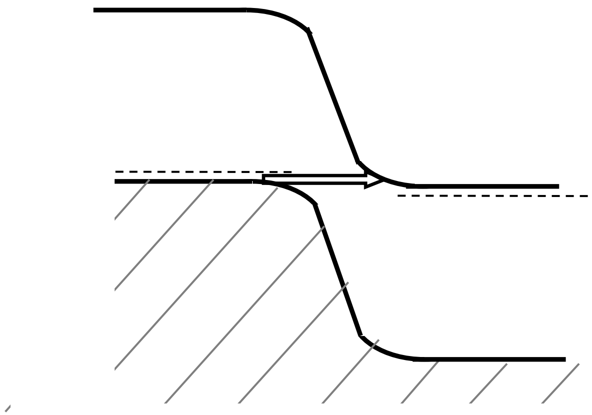
What could go wrong?

1. quantum-mechanical level repulsion:

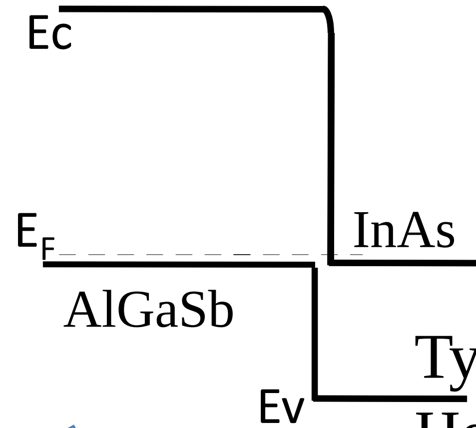


levels never line up!

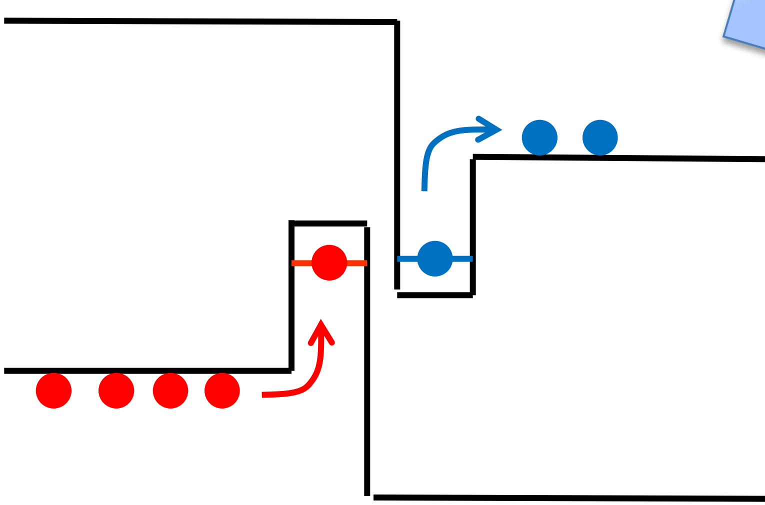
Evolution of the Tunnel Switch 2010-2012:



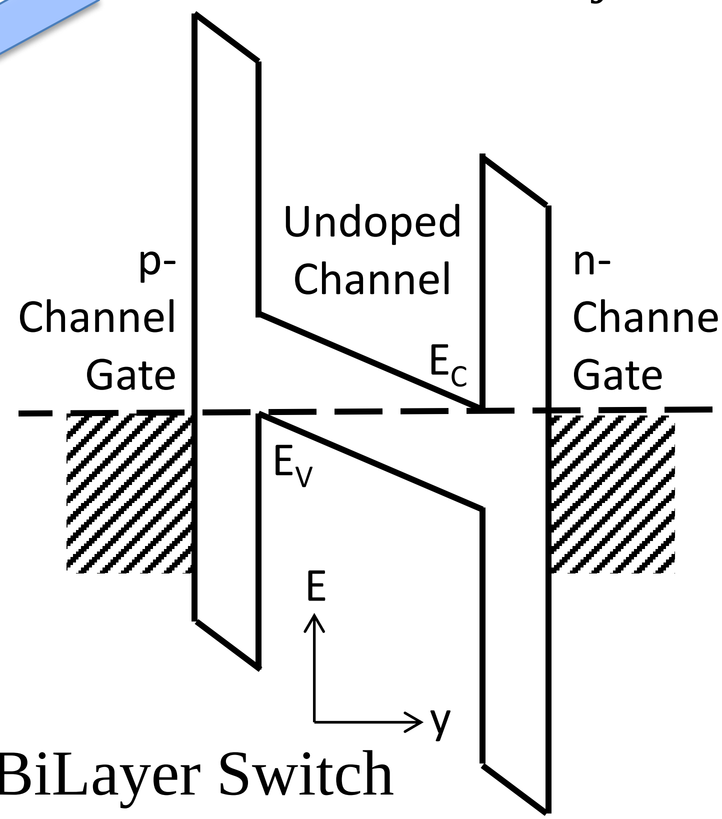
Homojunction Backward Diode



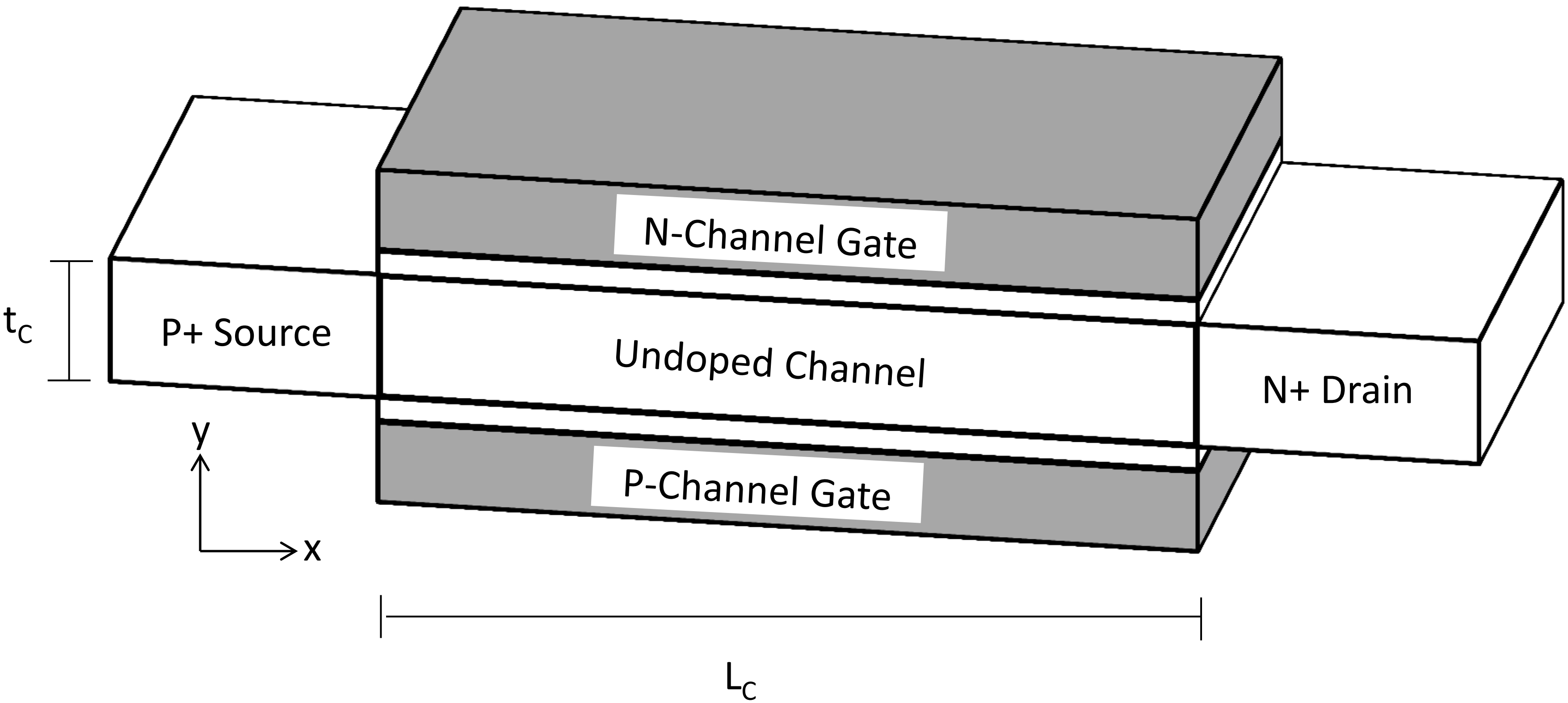
Type III Heterojunction

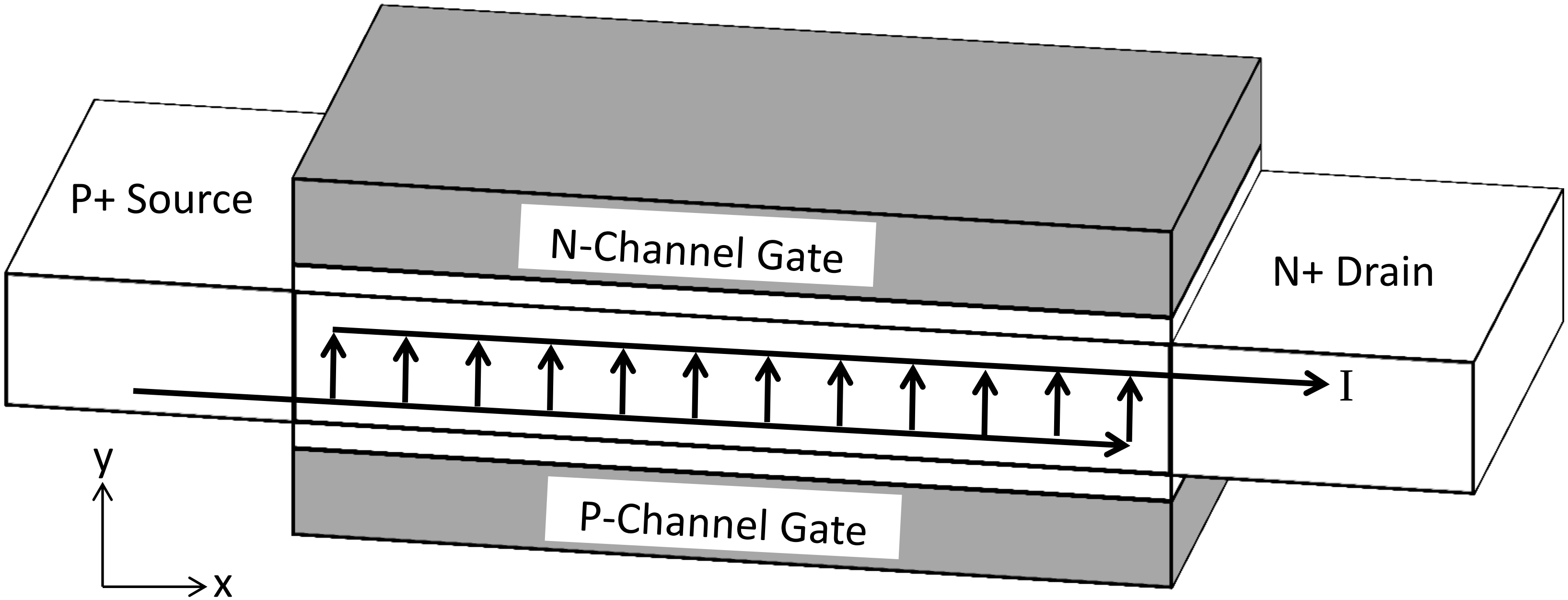


2d-2d pn Hetero-junction



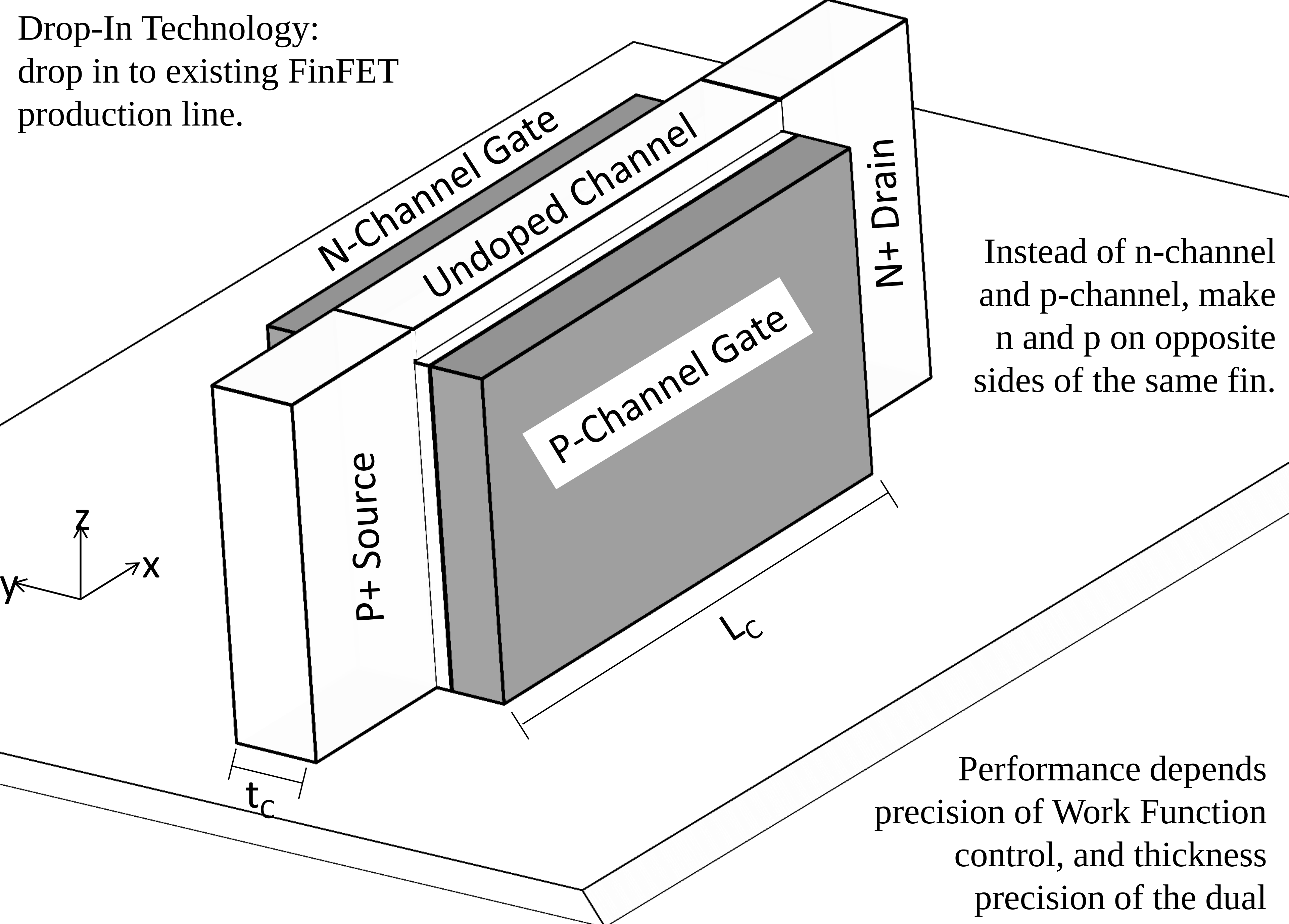
BiLayer Switch


N-Channel Gate
P+ Source
Undoped Channel
N+ Drain
P-Channel Gate
t_C
y
x
L_C



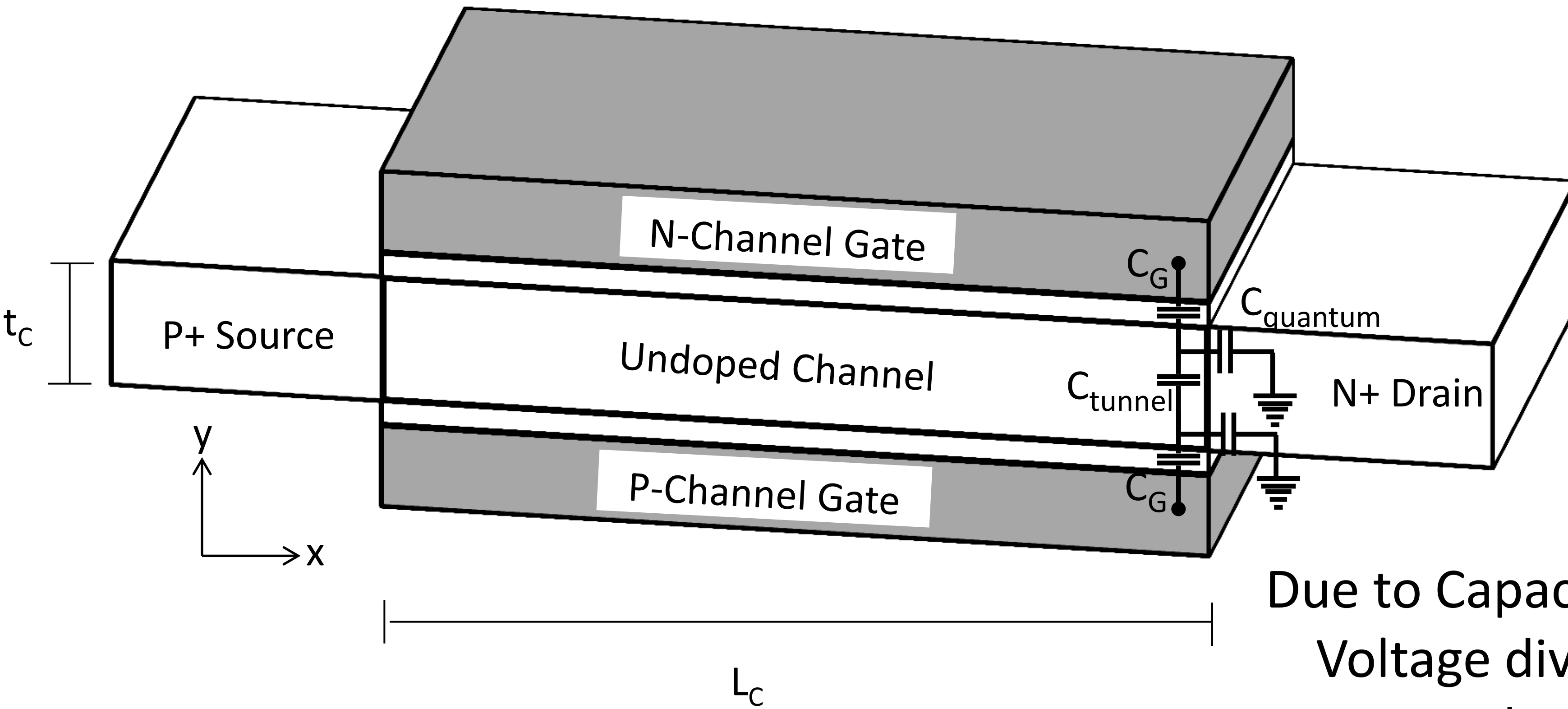
The Bi-Layer pn-junction or
the Bi-Layer Tunneling Field Effect Transistor

Drop-In Technology:
drop in to existing FinFET
production line.



Instead of n-channel
and p-channel, make
n and p on opposite
sides of the same fin.

Performance depends
precision of Work Function
control, and thickness
precision of the dual
channel layer.

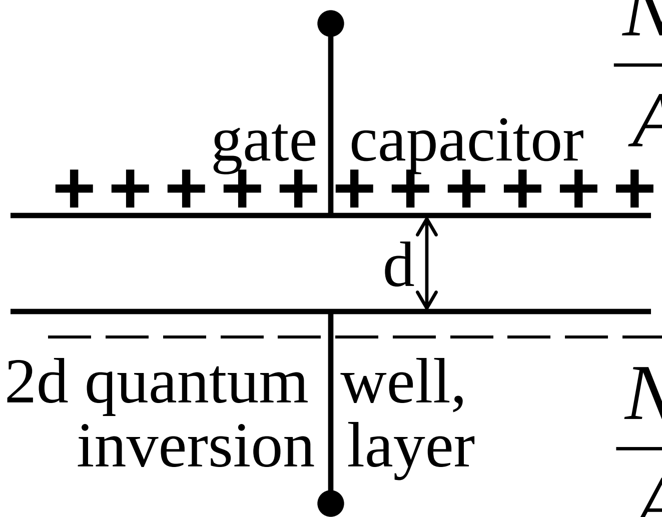


Due to Capacitive Voltage divider, the gate efficiency is poor, ~15% for a silicon fin

Quantum Capacitance impels small Effective Mass:

charge density on capacitor plate

$$\frac{N}{A} = \frac{\varepsilon_r \varepsilon_o}{qd} \frac{V}{d}$$



$$\frac{N}{A} = \frac{m^*}{\pi \hbar^2} qV$$

charge density of 2d density-of-states

Respectable gate efficiency requires: $\frac{qm^*}{\pi \hbar^2} < \frac{\varepsilon_r \varepsilon_o}{qd^2}$

Respectable gate efficiency requires $m^* < 0.1 m_o$

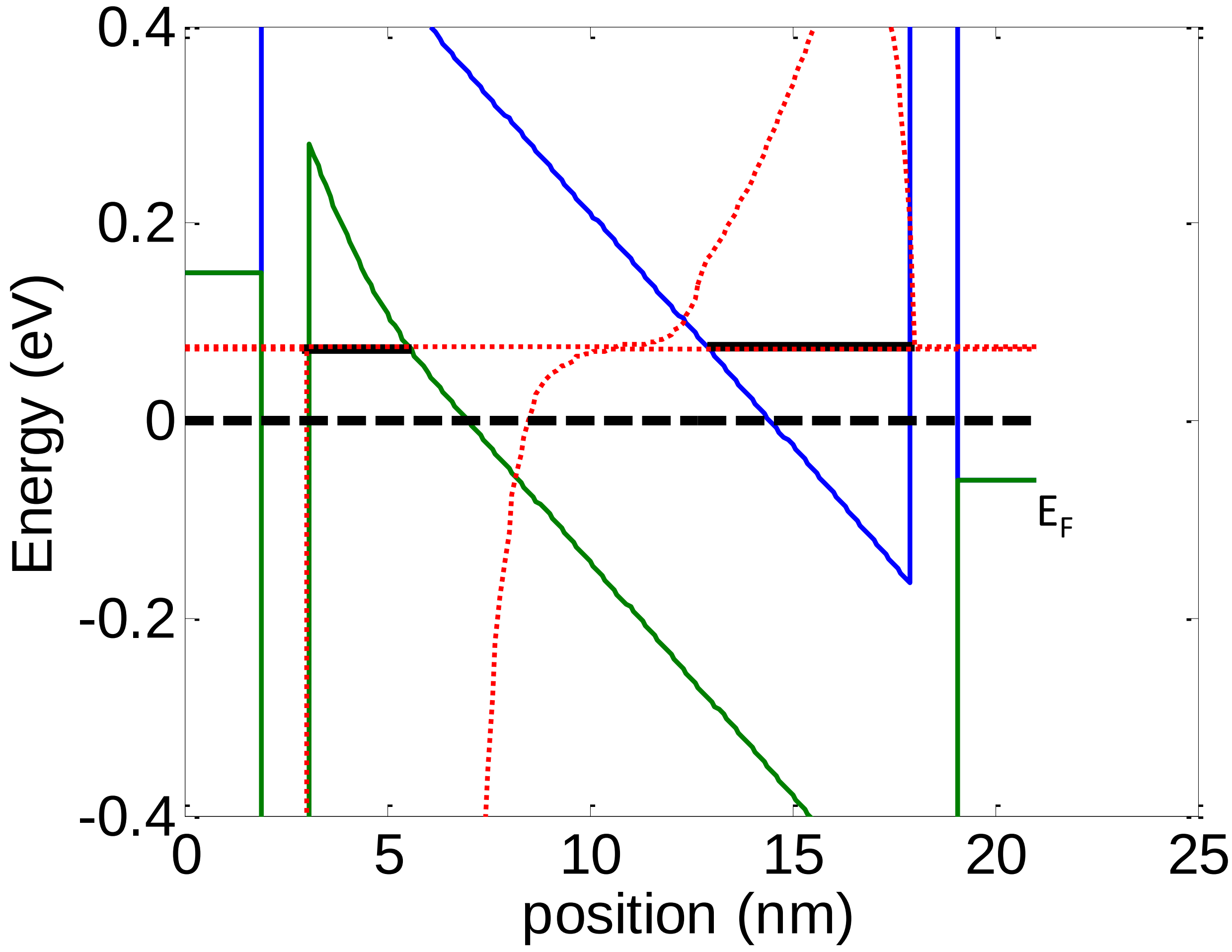
Try InAs,
effective mass is lower,
density of states is lower,
and $C_{quantum}$ is lower.

The lower n-channel carrier density makes it easier to swing the energy level

Lower effective mass—easier tunneling

We need $m_{eff}<0.1$

InAs Band Diagram at Turn-on



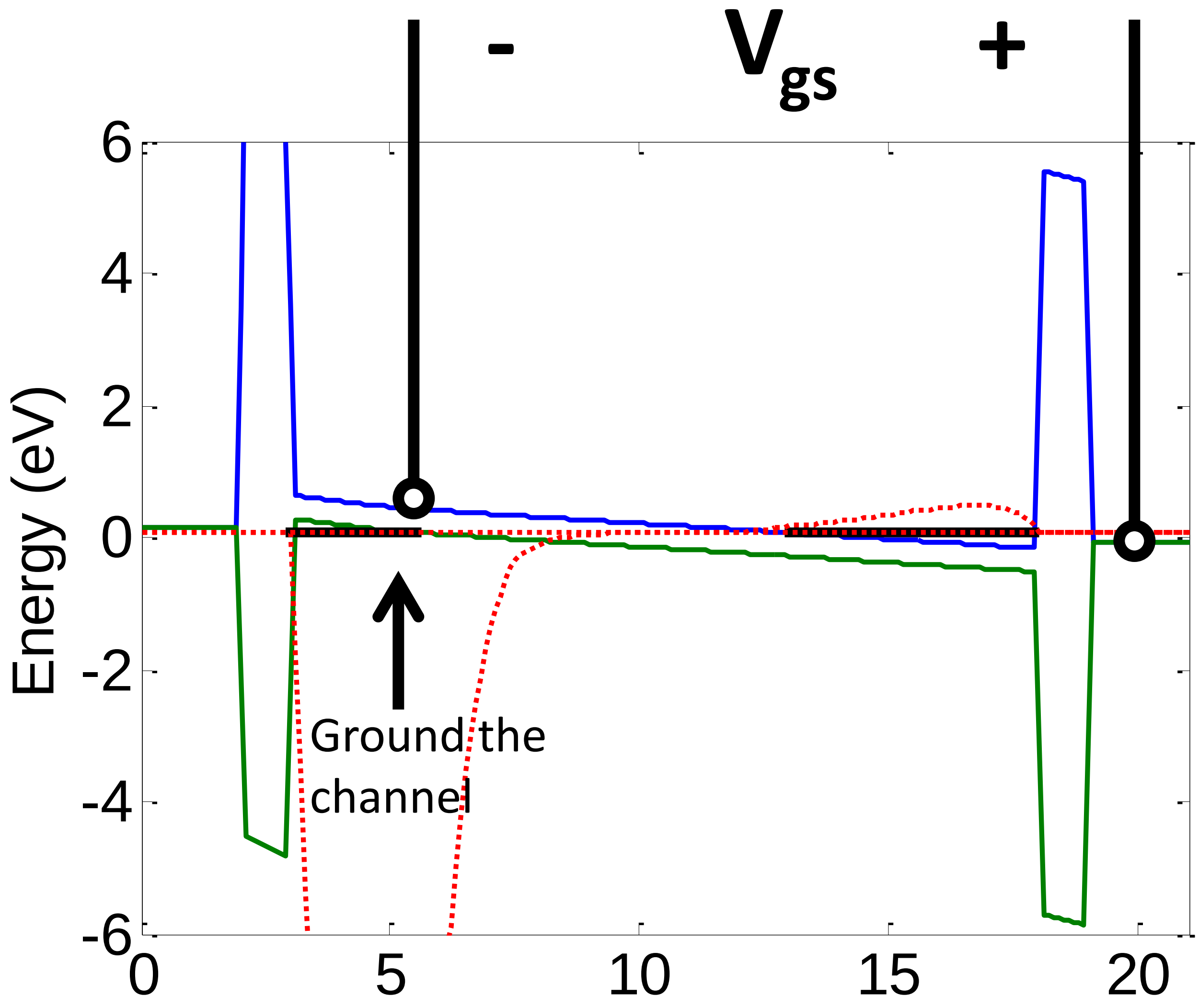
No Doping!

For Lab experiments: use Electric Field Induced pn junction.

For production use: Work Function induce pn junction.

InAs Asymmetric 15 nm Body

Ground the Valence Band Channel for better gate control on the n-channel



1 nm oxides

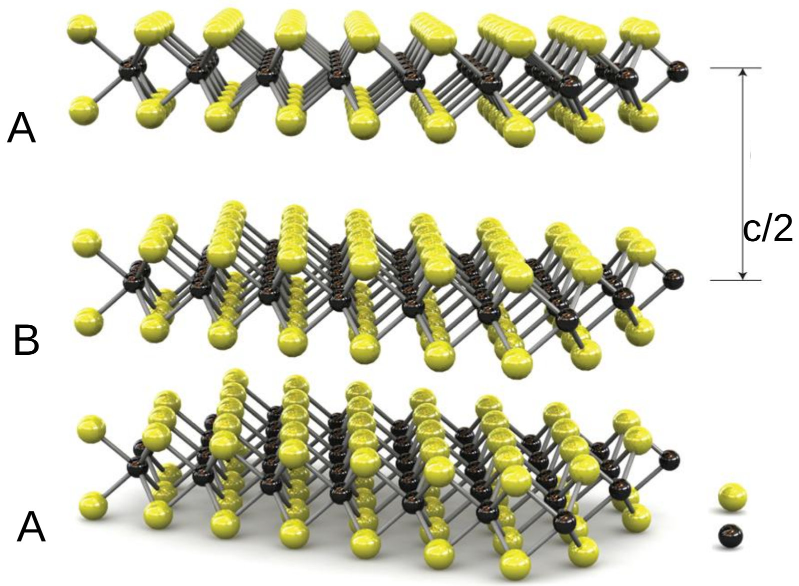
100 nm long channel length

Ground heavy hole band (heavy in the tunneling direction)

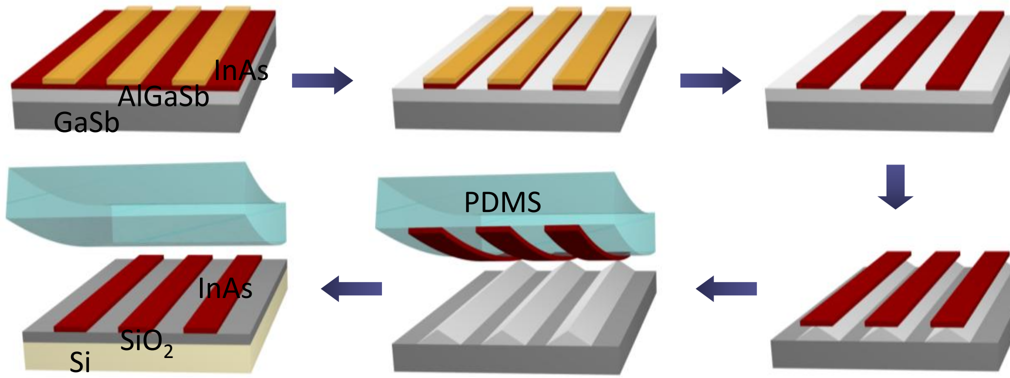
2D Nanomembranes for Novel Tunneling (A. Javey)

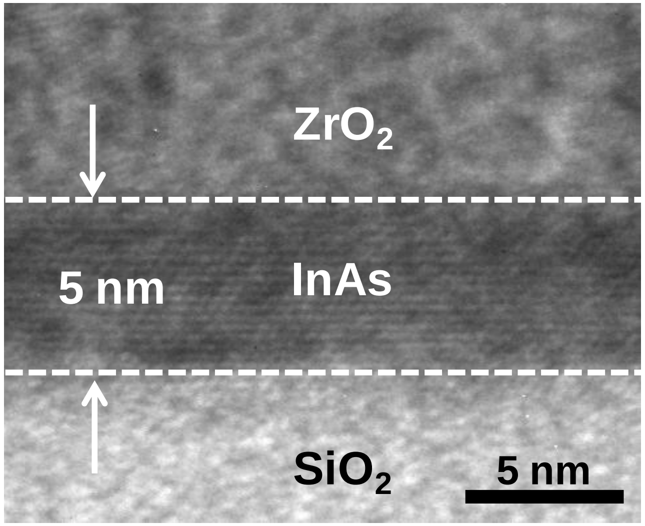
Layered Semiconductors

- ❑ **TMDC (eg. WSe_2, MoS_2)**,
- ❑ III-VI (eg. GaSe)

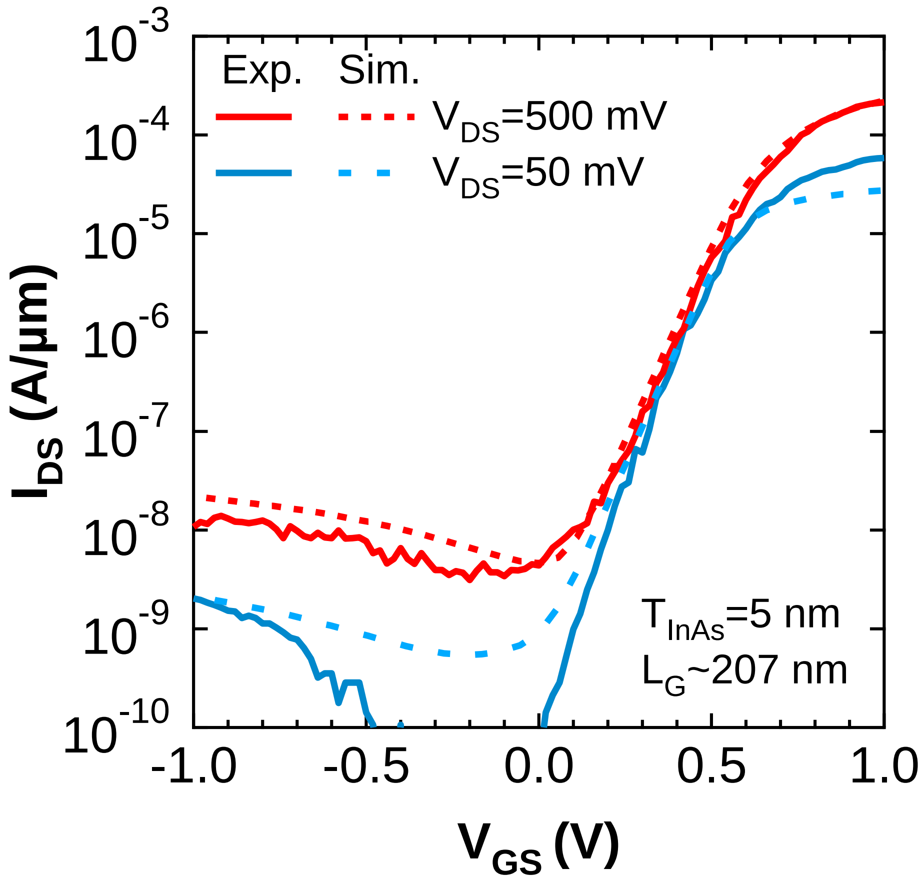


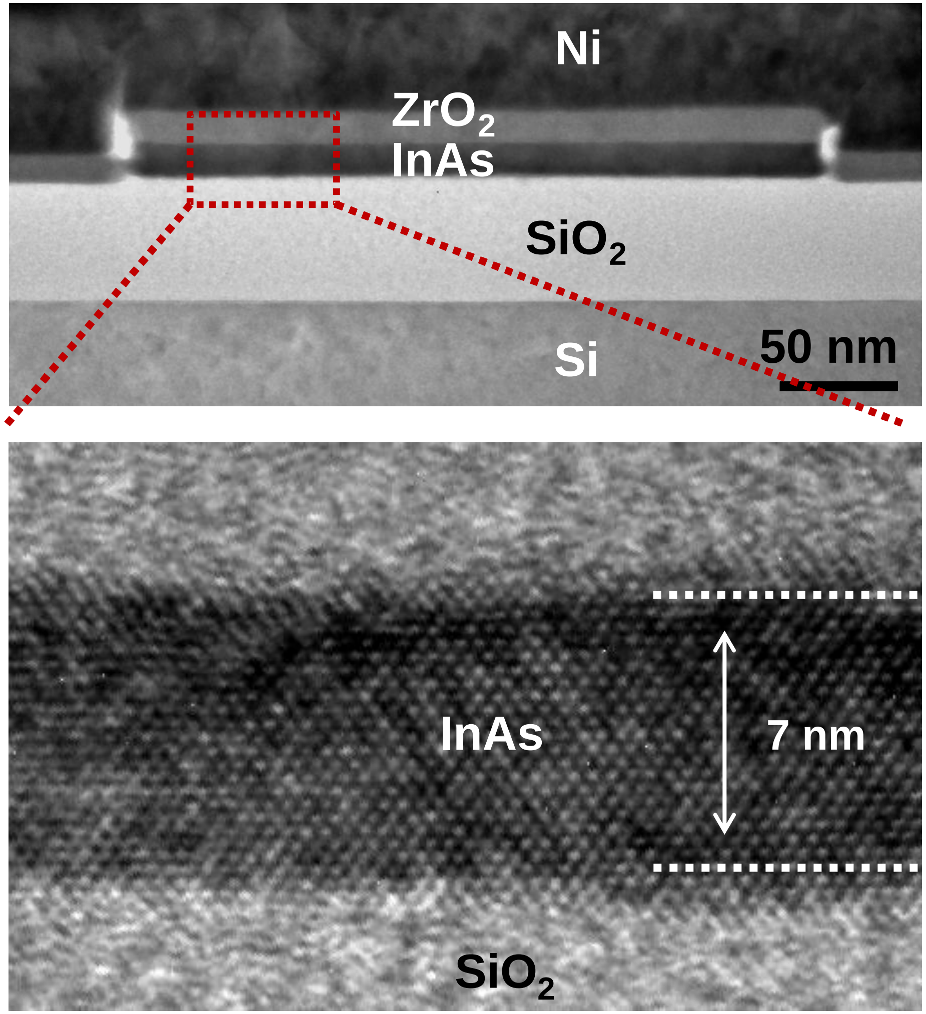
III-V on Insulator (XOI)





High Performance InAs XOI n-MOSFETs

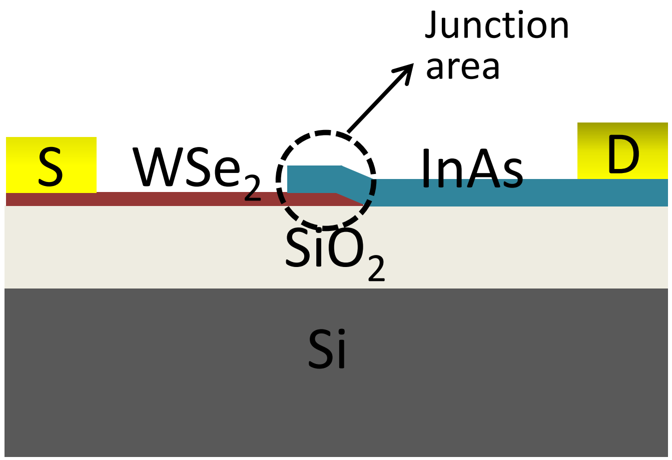


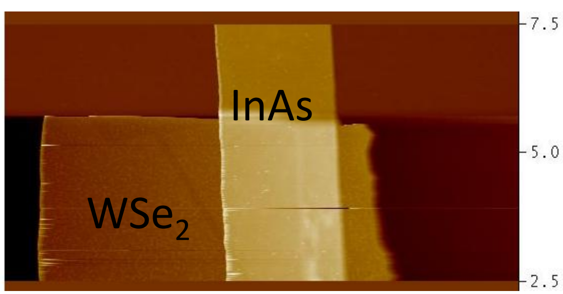


Electron Mobility: 1000-7000 cm^2/Vs
SS ~ 75 mV/decade
R_c~80 Ωμm

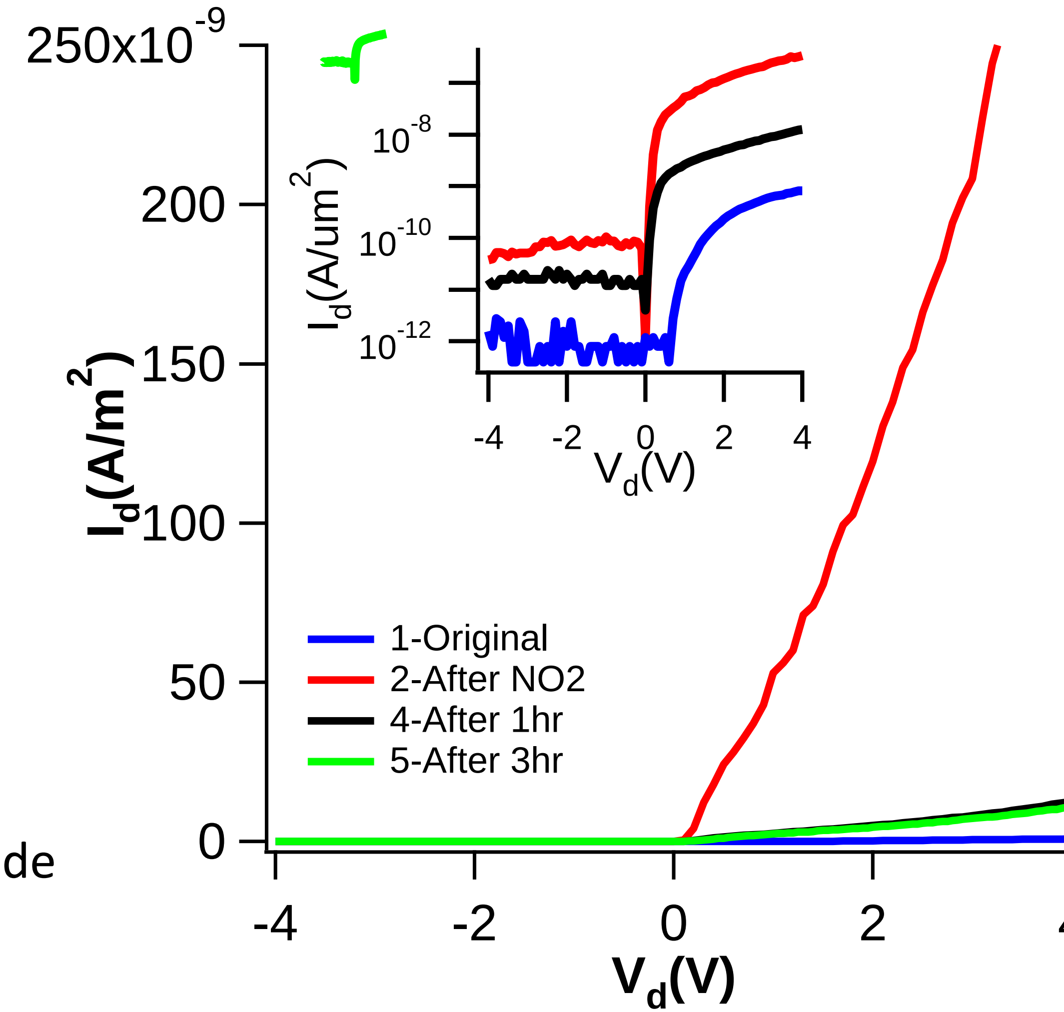
Kuni Takei, et al, Nano Letters, 2011.
Kuni Takei, et al, APL, 2011
H Ko, et al, Nature, 2010

InAs/WSe_2 Heterostructure





- ➢ First demonstration of a diode based on a van der Waals heterojunctions.
- ➢ Clear rectifying behavior is observed



Steven Chuang, et al, submitted, 2012

Materials Approach:

Van der Waals 2D membranes:

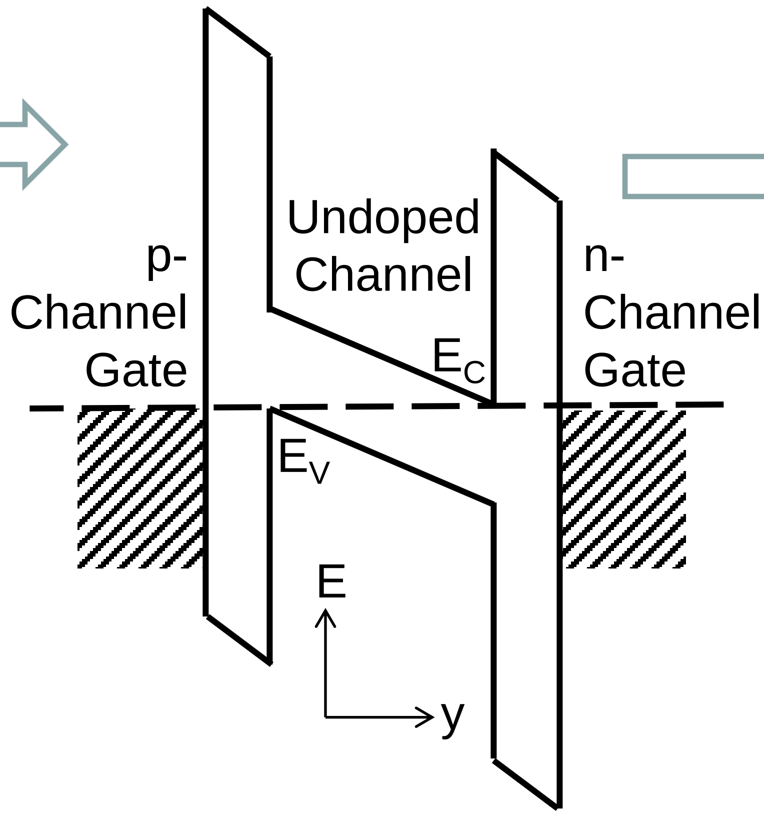
- ❑Removes lattice mismatch constraints
- ❑Mix and Match: A wide range of heterojunctions is available
- ❑Atomically abrupt interfaces

Roadmap:

Scientific

Research

Backward Diode



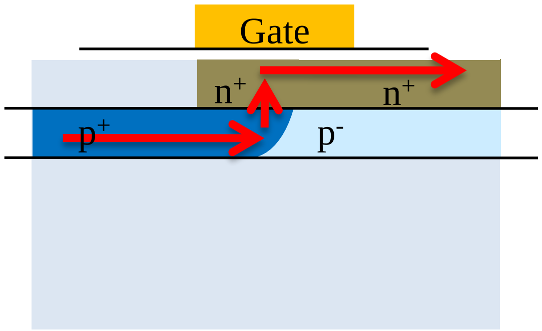
many analog applications:

Sensors

Photodetectors

radio mixers

TFET



MATERIALS:

InAs/GaSb

InAs

Fixed Layer Thickness $\left\{ \begin{array}{l} MoS_2 \\ WSe_2 \end{array} \right\}$ **Layered Chalcogenides**

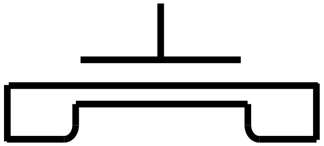
What keeps me up at night:

Band edges are simply not sharper than ~kT/3q,
allowing us to pick up only a factor ~3 improvement.

What doesn’t worry me:

Manufacturability and Yield.
If we can demonstrate individual high-performing devices, then a large international effort will become directed toward these problems.

A low-voltage technology, or an impedance matching device, needs to be invented/discovered at the Nano-scale:



transistor amplifier with steeper sub-threshold slope

- TFET's
- Negative Capacitance Gates

--VO_2 metal-insulator transition

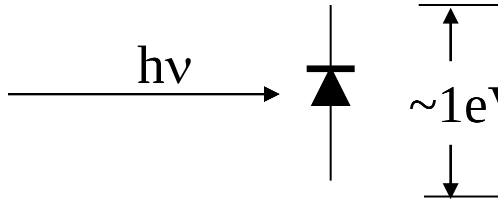
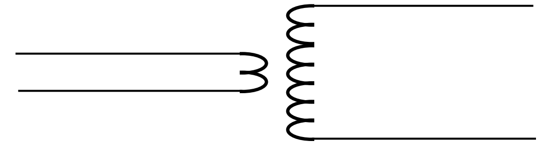
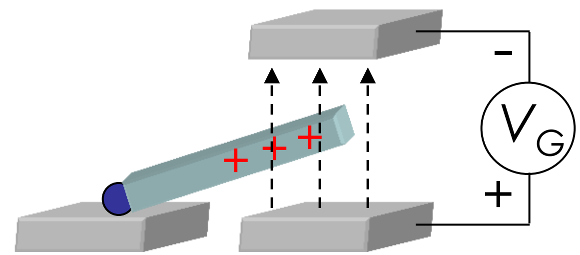


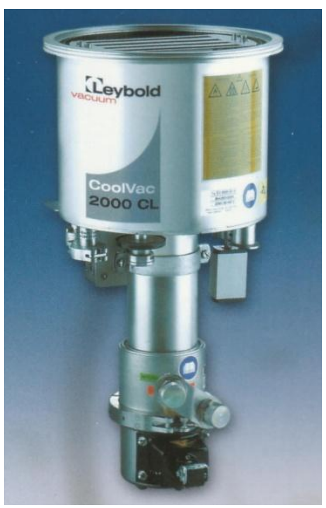
photo-diode



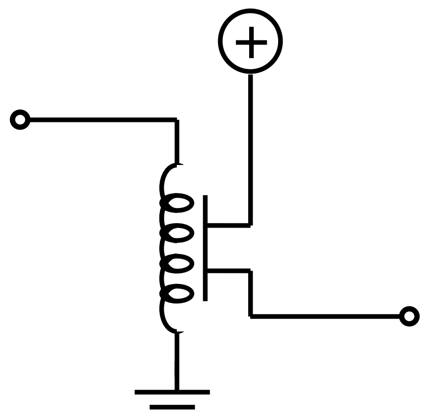
nano-transformer



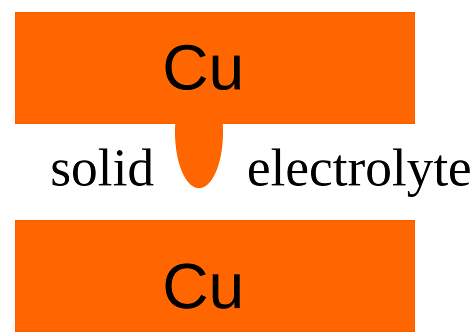
MEM's switch



Cryo-Electronics
kT/q~q/C



giant magneto-resistance
spintronics



Electro-Chemical Switch